

**LECTURE NOTES  
ON  
POWER ELECTRONICS**

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## **MODULE- I**

## POWER ELECTRONICS

Power electronics is partly belongs to Electrical Engineers and partly electronics Engineers. For Electrical Engineers is mainly concerned with generation, transmission and distribution and utilization of electric energy at high frequency.

Power electronics is subject that concerns the application of electronic principles into situation that are rated power level rather than signal level. The edge of modern power electronics began with the invention of silicon controlled rectifier (SCR) by Bell Laboratories in 1956. Its first prototype was introduced by GEC in 1957.

→ The term "converter system" is used to denote a static device that converts ac to dc, dc to ac, dc to dc. conventional power controller based on thyristors, mercury arc rectifier, magnetic amplifier, electrostatic controllers etc have been replaced by power electronics controllers using semiconductor devices in almost all applications.

Applications :- (i) HVDC voltage transmission, excitation system, VAR compensation,

(ii) Battery charger, traction control of electric vehicles, electric locomotives, street car, trolley buses, subway automatic electronics.

Advantages : High efficiency due to low loss in power semiconductor devices.

- (i) High reliability of power-electronic converter system
- (ii) Fast dynamic response of the power electronic

system as compared to electromechanical converter system.

Disadvantages power-electronic converter circuit have a tendency to generate harmonics in the supply system as well as in the load circuit.

- (ii) AC to DC and AC to AC converters operates at low input PF under certain operating conditions. In order to avoid a low PF, some special measures have to be adopted.
- (iii) Power electronics converters have low overload capacity.
- (iv) Regeneration of power is difficult in power electronics converter system.

Power Semiconductor devices:

Power diodes: - It is available up to 3000V, 350A, 1kHz

Thyristors - 6000V, 3500A, 1kHz

SI TH<sub>2</sub> (static induction Thyristors) 4000V, 220A, 20kHz

GTO (gate-turn off thyristors) 4000V, 3000A, 10kHz

MCT (MOS controlled thyristor) 600V, 60A, 20kHz

BJT - 1200V, 400A, 10kHz

power MOSFET and SET: - 1000V, 50A, and 1200V<sub>3rd</sub>

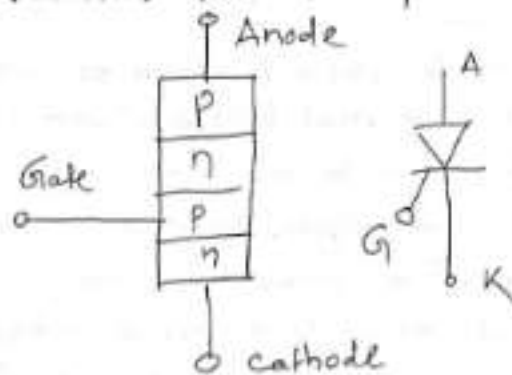
IGBT - 1200V, 400A, and 20kHz

SCR, GTO, SI TH<sub>2</sub> and MCT required pulse-gate signal for turning on, once these device are on, gate pulse is removed. But BJT, MOSFET, IGBT, and SET required continuous signal for keeping them in turn-on state.

# Thyristors

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Bell Laboratories were first developed silicon based semiconductor device. It was first developed by GEC (USA) in 1957. The word thyristor has become more synonymous with SCR. A thyristor has characteristic similar to a thyatron tube. But from the constructional point of view, thyristor belongs to transistor family (PNP or NPN devices). The name thyristor is derived by a combination of two words, THYatron and transISTOR. This means that thyristor is a solid state device like transistor and has characteristic similar to that thyatron tube.



Thyristor is a four layer three junction, three terminal semiconductor device. It has three terminals anode, cathode and Gate. The terminal connected outer P-layer is called anode and terminal connected outer n-layer is called cathode. The terminal connected inner

P-layer is called Gate. An SCR is so called because silicon is used for its construction and operation as a rectifier having low resistance in the forward conduction mode and having high impedance in the reverse direction can be controlled. It is similar to the diode, as SCR is an unidirectional device that blocks the flow from cathode to anode.

### V-I Characteristics:-

There are three different modes of conduction

- (a) Reverse blocking mode
- (b) Forward conduction mode
- (c) Forward blocking mode.

### Reverse blocking mode:-

When cathode is made positive with respect to anode, the thyristor is reverse biased. Junction  $J_1$ ,  $J_3$  are seen to be reverse biased, whereas junction  $J_2$  is forward biased. The device behaves as if two diodes are connected in series with reverse voltage applied across them. If the reverse voltage is increased, then at a critical breakdown level, called reverse breakdown voltage  $V_{BR}$ , gives rise to more losses in the SCR. The applied reverse voltage across thyristor is less than  $V_{BR}$ , the device offers a high impedance in the reverse direction.

Forward blocking mode :- When anode is positive with respect to cathode, with gate circuit open, the thyristor is said to be forward biased. The junction  $J_1$  and  $J_3$  are forward biased while junction  $J_2$  is reverse biased. In this mode, a small current called forward leakage current. When forward voltage is less than  $V_{BO}$ , SCR offers a high impedance. The thyristor can be treated as open switch.

Forward conduction mode :- In this mode, thyristor conducts current from anode to cathode with very small voltage drop across it. When anode to cathode voltage exceeding the forward breakover voltage or by applying gate pulse between gate and cathode, the thyristor is said to be forward bias. The on state voltage drop across p-n-n layers is in the order of 1 to 2 V.

Turn-on mechanisms :-

There are many methods available how to turn on the thyristor.

- (a) Forward voltage triggering :- When anode to cathode voltage is increased with gate circuit is open the reverse biased junction  $J_2$  will have avalanche breakdown at a voltage called forward breakover voltage  $V_{BO}$ . At this voltage, thyristor changes from off state to on state which characterised by low voltage across it with large forward current.

(b) Temperature Triggering: - During forward blocking mode, most of the applied voltage appears across reversed biased junction  $J_2$ . This voltage across junction  $J_2$  associated with leakage current may raise the temperature of the junction. With increase in temperature, the leakage current through the junction  $J_2$  increases. This is cumulative process may turn on the SCR at some high temperature.

(c) Light Triggering: - When high intensity of light such as neutrons or photons is focused on junction  $J_2$ , electron-hole pairs are generated in the device, thus increasing the number of charge carriers. This lead to instantaneous flow of current within the device and triggers the SCR. Such device is known as light activated silicon controlled rectifier (LASCR)

(d)  $\frac{dV}{dt}$  triggering: - With forward voltage across the anode and cathode of the device, the junction  $J_1$  and  $J_3$  are forward biased, whereas junction  $J_2$  has characteristic a capacitor due to charge existing across junction.

$$i = \frac{dQ}{dt} = \frac{d}{dt}(C_j V) = C_j \frac{dV}{dt} + V \frac{dC_j}{dt}$$

The rate of change of junction capacitance may be negligible as the junction capacitance is constant.

$$i = C_j \frac{dV_a}{dt}$$

If the  $\frac{dV_a}{dt}$  is large, the charging current is low.

The charging current plays an important role for bringing down the junction  $J_2$ .

Gate triggering:— When turn-on of a thyristor is required, a positive gate voltage between gate and cathode is applied. By gate current, charges are injected into the inner layer and voltage at which forward breakover voltage is reduced. The forward voltage at which the device switches to on state depends upon the magnitude of Gate current, higher the magnitude of gate current, lower is the forward breakover voltage.



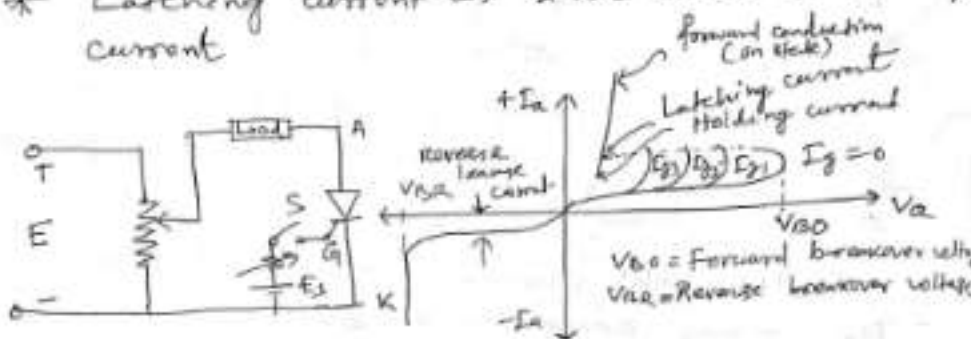
- \* Typically gate current magnitude of the order of 20 to 200mA
- \* No gate current is required for the device to remain in on state.

- \* If the gate current is reduced to zero before the rising anode current attains a value called Latching current, the device will turn-off.
- \* The magnitude of forward and reverse breakover voltage are nearly same and both are temperature dependent. In practice  $V_{BR}$  is slightly more than  $V_{BO}$ .
- \* The forward breakover voltage is taken as the final voltage rating of the device during the design of SCR applications.

Latching current:— The latching current may be defined as the minimum value of anode current which it must attain during turn-on process to maintain conduction when gate signal is removed.

Holding current:- Holding current may be defined as the minimum value of anode current below which it must fall for turning off the thyristor.

- \* The latching current is higher than the holding current
- \* Latching current is associated with turn-on process and holding current is associated with turn-off process.
- \* Latching current as 2 to 3 times the holding current



Gate characteristics :-

Gate-cathode circuit of  $V_{gm}$  a thyristor is a p-n junction, gate characteristic of the device are similar to that of diode. The spread, or scatter of gate characteristics is due to difference in the low doping level of p and n layers. The gate trigger circuitry must be suitable designed to take care of this unavoidable scatter of characteristics

- Curve 1:- Lowest voltage value that must be applied to turn on the SCR
- Curve 2:- Highest possible voltage value that can be safely applied to gate circuit.

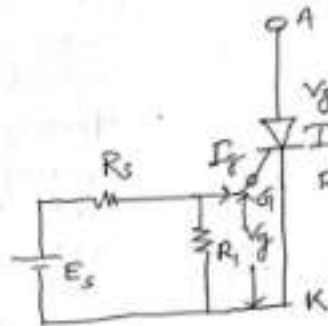
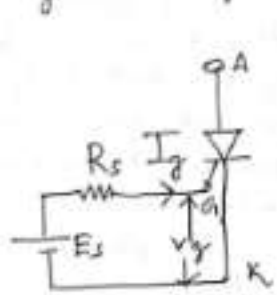
Each thyristor has maximum limits as  $V_{gm}$  for gate voltage and  $I_{gm}$  for gate current. There is also rated gate power dissipation  $P_{gav}$  specified for each SCR. These limits should not be exceeded in order to avoid permanent damage of junction  $J_2$ .

$I_{gmin}$ : - minimum value of gate current

$V_{gmin}$ : - minimum value of gate voltage

$V_{g0}$ : - Non-triggering gate voltage is also prescribed by the manufacturer.

\* Any unwanted signal is less than non-triggering gate voltage.



$E_s$  = gate source voltage  
 $V_g$  = gate-cathode voltage  
 $I_g$  = Gate current  
 $R_s$  = Gate-source resistor

$$E_s = V_g + I_g R_s$$

$$E_s = \left( I_{gmin} + \frac{V_{gmin}}{R_1} \right) R_s + V_{gmin}$$

\* A resistance  $R_1$  is also connected across gate-cathode terminal so as to provide easy path to flow of leakage current between SCR terminals.

$I_{gmin}$  and  $V_{gmin}$  are the minimum gate current and gate voltage to turn on SCR.

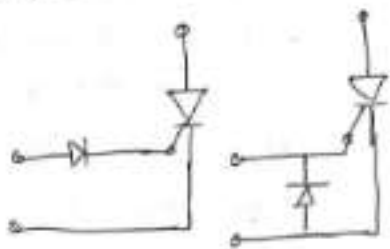
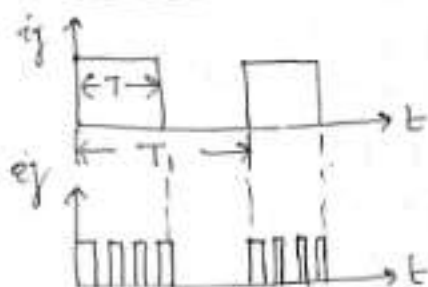
\* a. Thyristor is considered to be charge controlled device.

\* b. Higher the magnitude of gate current pulse, lesser is the time to inject the required charge for turning-on the thyristor.

\* SCR turn-on time can be reduced by using gate current of higher magnitude.

\* Gate Pulse width is usually taken as equal to or greater than SCR turn-on time.

$$\boxed{T \gg t_m} \quad T = \text{Pulse width.}$$



$$P_{gav} = \frac{1}{T_i} \int_0^T P_{gms} dt$$

$$P_{gav} = \frac{1}{T_i} P_{gms} T$$

$$\frac{P_{gav} T_i}{T} = P_{gms}$$

$$\boxed{\frac{P_{gav}}{fT} \leq P_{gms}}$$

$$\frac{P_{gav}}{\delta} \leq P_{gms}$$

$$\delta = \frac{T}{T_i} = fT$$

$$\delta = \text{duty cycle}$$

\* This type of technique of firing the thyristor is called high-frequency carrier gating. The advantages offered by this method of firing the SCR are lower rating, reduced dimension and therefore overall economical design of the pulse transformer.

\* The function of pulse transformer for isolating the low power circuit from main power circuit.

\* A diode is connected either in series with gate circuit or across gate-cathode terminal for preventing negative gate current.

Problem :- The trigger circuit of a thyristor has a source voltage of 15V and load line slope of 120V per ampere. The minimum gate current to turn-on the SCR is 25 mA. compute

- (a) source resistance required in the gate circuit  
 (b) The trigger voltage and trigger current for an average gate power dissipation of 0.4 watt.

Solution

$$V_g I_g = 0.4$$

$$E_s = R_s I_g + V_g$$

$$15 = 120 I_g + \frac{0.4}{I_g}$$

$$15 I_g = 120 I_g^2 + 0.4$$

$$I_g = 38.56 \text{ mA or } 86.44 \text{ mA}$$

$$120 I_g^2 - 15 I_g + 0.4 = 0$$

$$V_g = \frac{0.4 \times 10^3}{38.56} = 10.37 \text{ V}$$

$$\frac{0.4 \times 10^3}{86.44} = 4.627 \text{ V}$$

Choose  $V_g = 4.627 \text{ V}$  and  $I_g = 86.44 \text{ mA}$  of 25 mA. The slope of load line gives the required gate source resistance. From load line, series resistance in the gate circuit is  $120 \Omega$ .

Problem :- Latching current for an SCR inserted in between a dc voltage source of 20V and load is 100mA. Compute the minimum width of gate pulse current required to turn-on this SCR in case the load consists of (a)  $L = 0.2 \text{ H}$  (b)  $R = 20 \Omega$  in series with  $L = 0.2 \text{ H}$  (c)  $R = 20 \Omega$  in series with  $L = 2.0 \text{ H}$ .

Solution :-  $E = L \frac{di}{dt}$      $di = \frac{E}{L} dt$      $i = \frac{E}{L} t$

$$100 \times 10^{-3} = \frac{20 \text{ V}}{L} t \quad \text{or } t = \frac{0.1 \times 0.2}{L} = 100 \mu\text{sec.}$$

(b)  $E = Ri + L \frac{di}{dt}$      $i = \frac{E}{R} (1 - e^{-R/Lt})$      $0.100 = \frac{20 \text{ V}}{20} (1 - e^{-20/Lt})$      $t = 100.503 \mu\text{sec}$

(c)  $i = \frac{E}{R} (1 - e^{-R/Lt})$      $0.1 = \frac{20 \text{ V}}{20} (1 - e^{-20/Lt})$      $\text{or } t = 1005.03 \mu\text{sec.}$

## Switching characteristics during 'turn-on'

The time variations of the voltage across a thyristor and the current variation during turn on and turn-off process gives dynamic or switching characteristic of a thyristor.

- \* The turn-on time is defined as the time during which it changes from forward blocking state to forward conduction state. The total turn-on time can be divided into three intervals

(i) Delay time  $t_d$  (ii) Rise time  $t_r$  (iii) Spread time  $t_p$

Delay time :- The delay time  $t_d$  is measured from the instant at which gate current reaches  $90\% I_g$  to  $10\% I_a$ . As gate current begins to flow from gate to cathode with the application of gate signal, the gate current has non-uniform distribution of current density over the cathode surface due to p-layer. Its value is higher near the gate but decreases rapidly as the distance from the gate increases. During this period, anode current flows in a narrow region near the gate where gate current density is the highest. The delay time is fraction of  $t_{rec}$ .

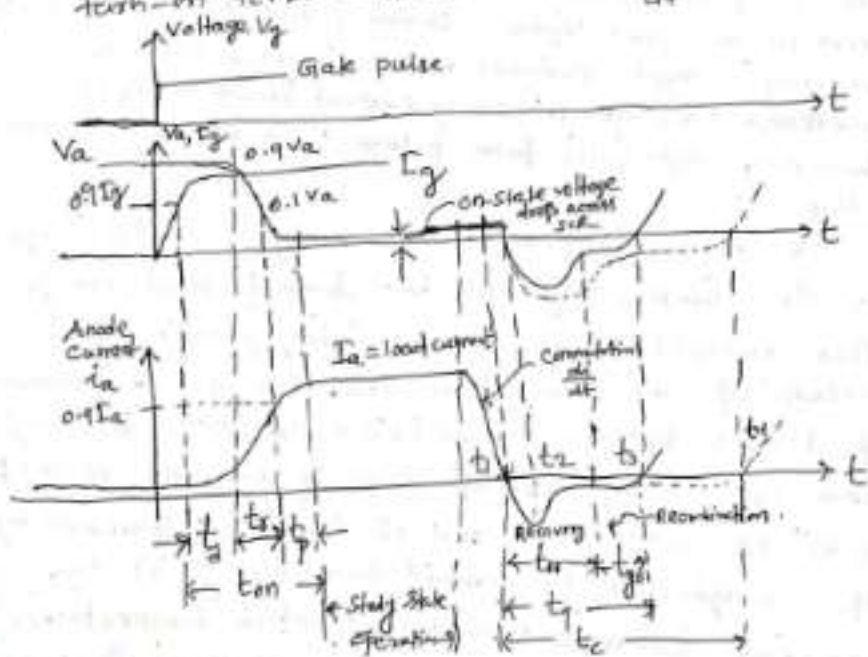
Rise time :- The rise time  $t_r$  is the time taken by the anode current to rise from  $0.1 I_a$  to  $0.9 I_a$ . The rise time is inversely proportional to the magnitude of gate current and its build up rate. So  $t_r$  can be reduced if high and steep current pulse are applied to the gate.

- \* For series R-L circuit, the rate of rise of anode current is slow,  $t_r$  is more.
- \* For R-C circuit,  $di/dt$  is high,  $t_r$  is less.

Spread time :- The spread time is the time taken by the anode current to rise from  $0.9 I_a$  to  $I_a$ . During this period conduction spreads over entire cross section of the cathode of SCR. The spreading interval depends on the area of cathode and gate structure of SCR. After spread time anode current attains steady value and voltage drops

across SCR is equal to on-state voltage drop of the order of 1 to 1.5V

- The turn on time usually order of 2 to 4  $\mu$ sec.
- \* Turn-on time depends upon anode circuit parameters and gate signal wave shape
- \* SCR is considered to be charge controlled device.
- \* Higher the magnitude of gate current, lesser time to inject this charge.
- \* The magnitude of gate current usually 3 to 5 times the minimum gate current required to trigger an SCR.
- \* Hard-firing or overdriving of a thyristor reduce its turn-on time and enhance the  $\frac{di}{dt}$  capability



Switching characteristic during turn-off: -

- The dynamic process of the SCR from conduction state to forward blocking state is known commutation or turn-off process

The turn-off time  $t_q$  of thyristor is defined as the time between the instant anode current becomes zero and the instant SCR regains forward blocking capability. During this period all the excess carriers from the four layers of SCR must be removed. During turn-off process holes from p-layer and electrons from n-layer must be removed. The carriers around junction  $J_2$  can be removed by the process of recombination.

The turn-off time is divided into two intervals.

- (a)  $t_{rr}$  (reverse recovery time)  
(b)  $t_{gr}$  (gate recovery time)  $t_q = t_{rr} + t_{gr}$

At time  $t_1$ , anode current becomes zero. After  $t_1$ , anode current flows in the reverse direction due to carriers stored in the four layers. During period  $(t_1 - t_2)$ , the reverse recovery current removes excess carriers from the end junctions. Reverse recovery current flows due to sweeping out holes from p-layer and electrons from n-layer.

At the end of reverse recovery period  $t_2 - t_1$ , the middle junction  $J_2$  still has some trapped charge. This trapped charge must be decay only by the process of recombination. The time for the recombination of charges between  $t_2$  and  $t_4$  is called gate recovery time  $t_{gr}$ . The turn-off time  $t_q$  is in the range of 3 to 100  $\mu$ sec. The turn-off time is influenced by the magnitude of forward current,  $\frac{di}{dt}$  at the time of commutation and junction temperature.

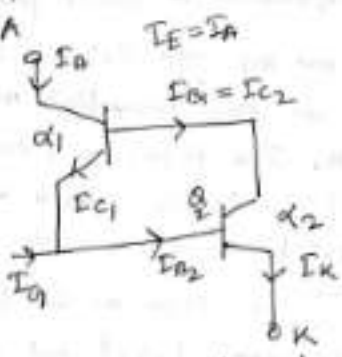
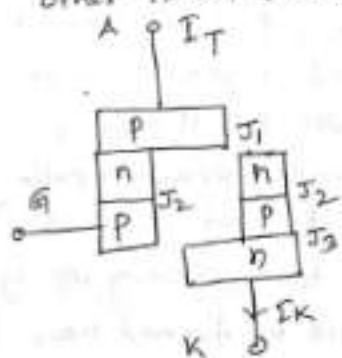
An increase in the magnitude of these factors increase the thyristor turn-off time. The turn-off time decreases with an increase in the magnitude of reverse voltage. The circuit turn-off time is defined as the instant anode current becomes zero and the instant reverse voltage due to practical ckt reaches zero.

Time  $t_c$  must be greater than  $t_{off}$  for reliable turn-off otherwise the device may turn-on at an undesired instant, a process called commutation failure.

- \* Thyristor turn-off time (50-100  $\mu$ s) converter grade SCR
- \* Thyristor turn-off time (3-50  $\mu$ s) inverter grade SCR.

## TWO TRANSISTOR MODEL OF THYRISTOR

The regenerative or latching action due to positive feedback can be realised by two transistor model. A thyristor can be considered as two transistors, one P-N-P transistor  $Q_1$  and other n-P-N transistor  $Q_2$ .



The relation between collector current and emitter current  $I_E$  and the leakage current of the collector base junction  $I_{CBO}$

$$I_C = \alpha I_E + I_{CBO}$$

$$\alpha = \frac{I_C}{I_E} = \text{current gain}$$

for transistor  $Q_1$   $I_{C1} = \alpha_1 I_A + I_{CBO1}$

$$I_{C2} = \alpha_2 I_A + I_{CBO2}$$

$$I_A = I_{C1} + I_{C2} \dots \dots \dots \textcircled{1}$$

$$= \alpha_1 I_A + I_{CBO1} + \alpha_2 I_A + I_{CBO2}$$

$$I_K = I_{Q1} + I_A$$

$$I_A = \frac{\alpha_2 I_{Q1} + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

The current gain  $\alpha_1$  varies with emitter current  $I_{E1}$   
 $\alpha_2$  varies with  $I_{E2} = I_A + I_{G1}$   
 If  $I_{G1}$  is suddenly increased, then increased  $I_{E2}$  which  
 would increase  $\alpha_1$  and  $\alpha_2$ .  $\alpha_2$  depends on  $I_{E1}$  and  $I_{E2}$ .  
 If  $\alpha_1$  and  $\alpha_2$  would increase, could further increase  
 $I_{E1}$ . If there is a regenerative or positive feedback  
 effect. If  $\alpha_1 + \alpha_2$  is equal to 1, resulting large values  
 of anode current  $I_A$  and thyristor will turn on by small  
 gate current.

### Protection of SCR

$\frac{di}{dt}$  Protection: - under forward biased condition and is  
 turned on by gate pulse, conduction of anode current  
 begins in the immediate neighbourhood of gate-cathode  
 junction. The thyristor design permits the spread of  
 conduction to the whole area junction areas as rapidly  
 as possible. If the rate of rise of anode current  
 i.e.  $\frac{di}{dt}$  is large as compared to the spreading velocity  
 of carriers, local hot spot will be formed near  
 the gate cathode on account of high current density.  
 There may be increase temperature. Therefore, the rate  
 of rise of anode current at the time of turn on  
 must be kept below the specified limiting value.

\* The value of  $\frac{di}{dt}$  can be maintained below  
 acceptable limit by using small inductor, called  
 $\frac{di}{dt}$  inductor.

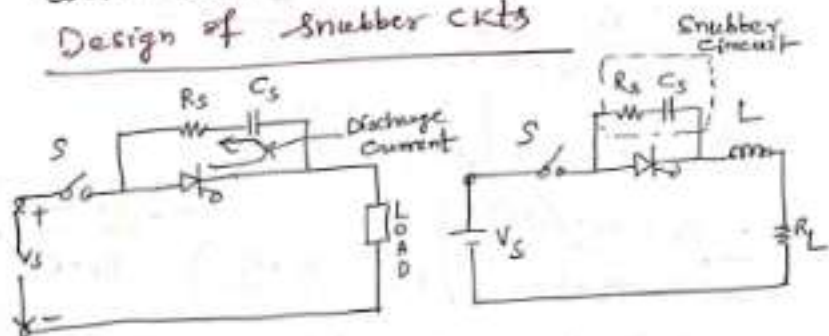
\* The  $\frac{di}{dt}$  limit value of SCR are 20-500 A/A.s

$\frac{dv}{dt}$  protection: — When forward voltage across the anode and cathode of a thyristor, the two outer junctions are forward biased but inner junction is reverse biased. The reverse biased junction has characteristics a capacitor. The charge existing that junction is  $Q$ .

$$i = \frac{dQ}{dt} = \frac{d}{dt}(C_j V_a) = C_j \frac{dV_a}{dt}$$

If the  $\frac{dv}{dt}$  is more, the charging current value will be more. The charging current play a major role for turning on the SCR even without gate signal is zero. Such Phenomena of turning on a Thyristor called  $\frac{dv}{dt}$  turn-on must be avoided as its leads to false operation of the thyristor circuit. Typical values of  $\frac{dv}{dt}$  are 20-500 V/μsec. Due to high value of  $\frac{dv}{dt}$ , the ~~the~~ thyristor may be false turn on which can be prevented by using "snubber" ckt in parallel with device.

### Design of Snubber CKTs



1. A snubber circuit consists of a series combination of resistance  $R_s$  and capacitance  $C_s$  in parallel with the thyristor. The purpose of capacitor connected in series with resistor is to prevent reversal  $\frac{dv}{dt}$ .

triggering of the SCR. When switch S is closed, capacitor behaves as short circuit, therefore the voltage across SCR is zero. After some time, the voltage across C<sub>s</sub> build up at slow rate. The  $\frac{dv}{dt}$  across C<sub>s</sub> and therefore SCR is less than the specified rating of the device. When SCR is turned on by gate pulse, capacitor C<sub>s</sub> discharge a current in reverse direction. This discharge current is limited by resistance R<sub>s</sub>. R<sub>s</sub>, C<sub>s</sub> and load circuit parameters form an underdamped circuit so that  $\frac{dv}{dt}$  is limited to acceptable values.

The design of snubber circuit parameters is quite complex and only approximate calculation is required.

Applying KVL to the snubber circuit

$$R_s i + R_L i + L \frac{di}{dt} = V_s$$

Laplace transformation.

$$(R_s + R_L) I(s) + L [s I(s) - I(0^+)] = \frac{V_s}{s}$$

$$(R_s + R_L + Ls) I(s) = \frac{V_s}{s}$$

$$I(s) = \frac{V_s}{s(R_s + R_L + Ls)} = \frac{A}{s} + \frac{B}{R_s + R_L + Ls}$$

$$A = \frac{V_s}{R_s + R_L} \Big|_{s=0}$$

$$B = \frac{V_s (R_s + R_L + Ls)}{s(R_s + R_L + Ls)} \Big|_{s = -\left(\frac{R_s + R_L}{L}\right)} = -\frac{V_s L}{R_s + R_L}$$

$$I(s) = \frac{V_s / R_s + R_L}{s} - \frac{V_s L / R_s + R_L}{R_s + R_L + Ls}$$

$$= \frac{V_s}{R_s + R_L} \left( \frac{1}{s} - \frac{L}{R_s + R_L + Ls} \right)$$

$$i(t) = \frac{V_s}{R_s + R_L} \left( 1 - e^{-t \frac{R_s + R_L}{L}} \right)$$

$$\frac{di}{dt} = \frac{V_s}{R_s + R_L} e^{-t \frac{R_s + R_L}{L}} \cdot \frac{R_s + R_L}{L}$$

$$= \frac{V_s}{L} e^{-\frac{R_s + R_L}{L} t}$$

$$\left. \frac{di}{dt} \right|_{\max} \text{ at } t=0$$

$$\boxed{\left. \frac{di}{dt} \right|_{\max} = \frac{V_s}{L}}$$

The voltage across SCR  $V_a = R_s \cdot i$

$$\frac{dV_a}{dt} = R_s \cdot \frac{di}{dt}$$

$$\left. \frac{dV_a}{dt} \right|_{\max} = R_s \cdot \left. \frac{di}{dt} \right|_{\max}$$

$$\boxed{\left. \frac{dV_a}{dt} \right|_{\max} = R_s \cdot \frac{V_s}{L}}$$

$$E(s) = \frac{V_s}{s} = R_s i(s) + L \frac{di(s)}{dt} + \frac{1}{C} \int i(s) dt = V_s$$

by Applying KVL

$$R_s I(s) + Ls I(s) + \frac{1}{Cs} I(s) = \frac{V_s}{s}$$

$$I(s) = \frac{V_s}{s(R_s + Ls + \frac{1}{Cs})} = \frac{V_s C/s}{s(R_s Cs + Lcs^2 + 1)} = \frac{V_s C}{R_s Cs + Lcs^2 + 1}$$

$$= \frac{V_s C/Ls}{s^2 + \frac{R_s Cs}{L} s + \frac{1}{LC}}$$

$$2\zeta \omega_n = \frac{R_s}{L}$$

$$2\zeta \cdot \frac{1}{\sqrt{LC}} = \frac{L}{L} \frac{R_s}{L}$$

$$\omega_n = \frac{1}{\sqrt{LC}}$$

$$\cos = \frac{1}{\sqrt{LC}}$$

$$26. \frac{1}{\sqrt{LC}} = \frac{R_s}{L}$$

$$25 \frac{1}{\sqrt{L}} \cdot \frac{1}{\sqrt{C}} = \frac{R_s}{L}$$

$$25 \frac{1}{\sqrt{C}} = \frac{R_s}{\sqrt{L}}$$

$$R_s = 25 \sqrt{\frac{L}{C}}$$

The damping factor in the range 0.5 to 1.

Problem:- A thyristor operating from a peak supply voltage of 400V has the following specifications.

Repetitive peak current  $I_p = 200A$   $\left(\frac{di}{dt}\right)_{max} = 50A/\mu sec$

$\left(\frac{dv}{dt}\right)_{max} = 200V/\mu sec$  choosing a factor of safety of 2.

For  $I_p$ ,  $\left(\frac{di}{dt}\right)_{max}$  and  $\left(\frac{dv}{dt}\right)_{max}$ . Design a suitable

snubber circuit. The minimum value of load resistance is  $10\Omega$ .

Solution:- For a factor of safety of 2, the permitted value

are  $I_p = \frac{200}{2} = 100A$   $\left(\frac{di}{dt}\right)_{max} = \frac{50}{2} = 25A/\mu sec$

$\left(\frac{dv}{dt}\right)_{max} = \frac{200}{2} = 100V/\mu sec$

$$L = \frac{V_s}{\left(\frac{di}{dt}\right)_{max}} = \frac{400 \times 10^{-6}}{25} = 16\mu H$$

$$R_s = \frac{L}{V_s} \cdot \left(\frac{dv}{dt}\right)_{max} = \frac{16 \times 10^{-6}}{400} \times \frac{100}{10^{-6}} = 4\Omega$$

The peak current through the thyristor is

$$\frac{400}{10} + \frac{400}{4} = 140A$$

This current is more than the permissible peak current of 100A. ~~The~~ The value of  $R_s$  is chosen

$$8\Omega \quad \frac{400}{10} + \frac{400}{8} = 90A$$

which is less than the allowable peak current

$$R_s = \sqrt[2]{\frac{L}{C_s}} \quad \gamma = 0.15$$

$$C_s = \left( \frac{2 \gamma}{R_s} \right)^2 \cdot L = \left( \frac{1.3}{8} \right)^2 \times 16 \times 10^{-6} = 0.4225 \mu\text{F} \quad (\text{Ans})$$

The value of  $C_s$  may be lowered so  $C_s$  may be taken  $0.3 \mu\text{F}$ .

$$i = C \frac{dv}{dt}$$

$$\frac{V_s}{R_s + R_L} = C \frac{dv}{dt} \quad \frac{400}{1+8} = 0.3 \times 10^{-6} \frac{dv}{dt}$$

$$\text{So, } \frac{dv}{dt} = \frac{400}{18} \times \frac{1}{0.3 \times 10^{-6}} = 74.07 \text{ V}/\mu\text{s}$$

Overvoltage protection:-

(a) Internal overvoltage:- Large overvoltage may be generated internally during commutation of thyristor. When anode current reduces to zero, large transient overvoltage will be produced. This voltage is several times larger than breakover voltage of the device, the thyristor may be destroyed permanently.

(b) External overvoltage.

→ Due to lightning strokes.

→ When thyristor converter is fed through transformer, voltage transients are likely to occur when the transformer primary is energized or de-energized. Such overvoltage may cause random turn-on of a thyristor.

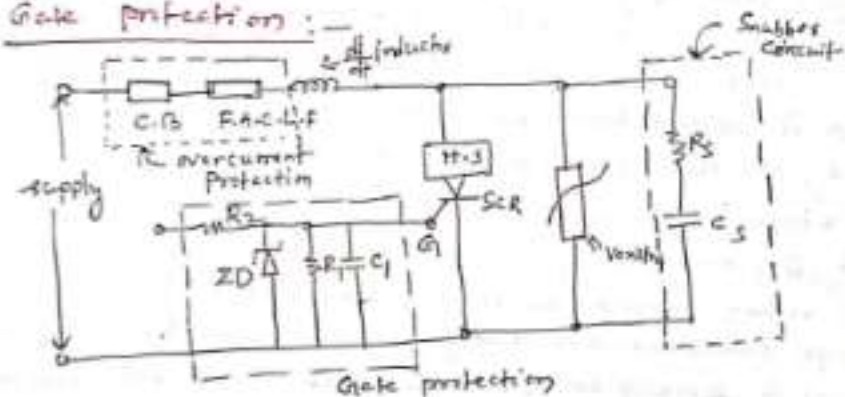
Suppression of overvoltage:-

- Non-linear resistor.
- Voltage clamping device.
- Snubber circuit is also helpful in damping overvoltage transient spikes for limiting  $\frac{dv}{dt}$  across thyristor.
- Selenium thyrector diode.
- Metal oxide varistor.
- avalanche diode suppressor.

## overcurrent protection:

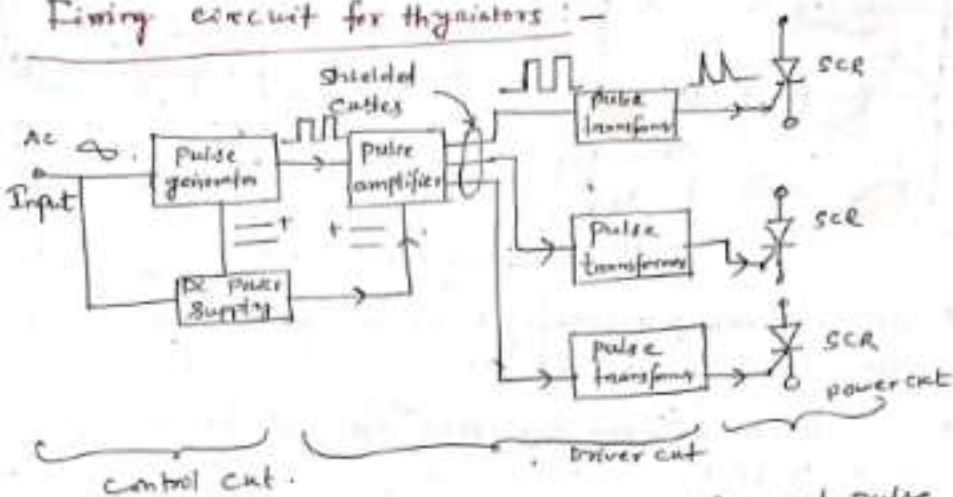
- Both circuit breakers and fast acting current-limiting fuse are used for protection SCR.
- A CB has long tripping time and also used for continuous overloads or against surge current for long duration.
- A F.A.C.L.F is used for protecting thyristor against large surge ~~rating~~ current of very first duration.
- Electronic Crowbar protection.

## Gate protection:



- The function of Zener diode is to protect against over voltage
- A resistor  $R_2$  is connected in series with gate circuit provides against overcurrent
- A capacitor and resistor are also connected across gate to cathode to bypass the noise signals.

## Firing circuit for thyristors :-



- Driver circuit consist of a pulse amplifier and pulse transformer.
- The function of pulse transformer is to isolate the low voltage gate-cathode circuit from high voltage anode-cathode circuit.

### R-triggering :-

$R_2$  = Variable resistance

$R$  = stabilizing resistance

$R_1$  = gate current limiting resistance

If  $R_2 = 0$  gate current flow from driving

Load,  $R_1$ , D and gate to cathode.

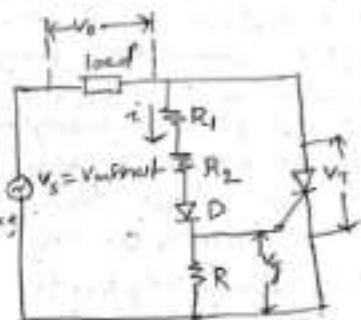
$$\text{So, } \frac{V_m}{R_1} \leq I_{gm} \quad \text{or } R_1 \geq \frac{V_m}{I_{gm}}$$

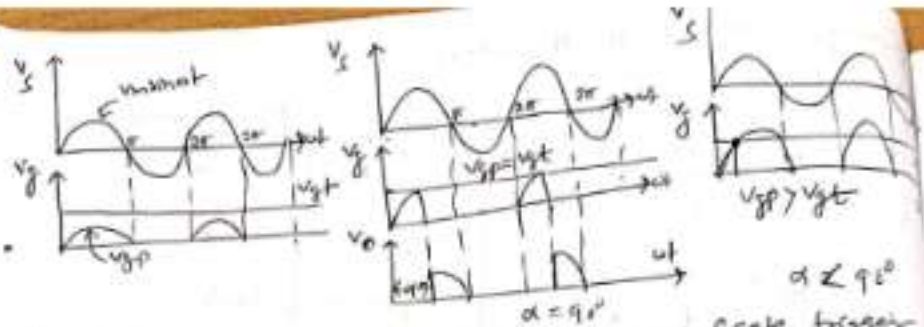
$V_m$  = maximum value of source voltage.

Resistance  $R$  should have such a value that maximum voltage drop across it does not exceed maximum possible gate voltage  $V_{gm}$

$$\frac{V_m}{R_1 + R} \leq V_{gm}$$

$$R \leq \frac{V_{gm} \cdot R_1}{V_m - V_{gm}}$$

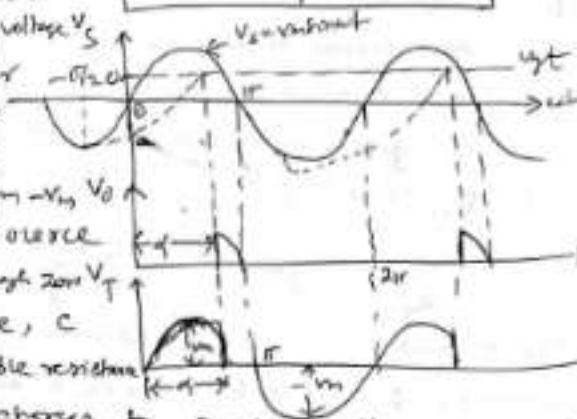
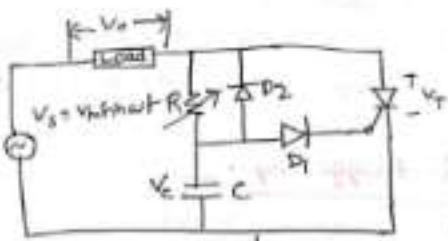




- If  $V_{gp}$  (Peak gate voltage) is less than  $V_{gt}$  (gate trigger voltage), SCR will not turn-on.
- If  $R_2$  is adjusted such that  $V_{gp} = V_{gt}$  for firing angle is  $90^\circ$ .
- The resistance triggering can not give firing angle below  $90^\circ$ .

R-C firing circuits:-

By varying the value of  $R$ , firing angle can be controlled from  $0^\circ$  to  $180^\circ$ . In the negative half cycle, capacitor  $C$  charges through  $D_2$  with less plate positive to peak supply voltage  $V_s$   $V_m$  at  $\omega t = -90^\circ$ . After source voltage crosses from  $-V_m$  to  $0$ . The capacitor voltage  $V_c$  from  $-V_m$   $V_0$  to  $(-\infty)$  at  $\omega t = 0^\circ$ . Source voltage passes through zero  $V_T$  and becomes positive,  $C$  charges through variable resistance  $R$ . When capacitor charges to positive voltage equal to gate trigger voltage  $V_{gt}$ , SCR will be fired. The diode  $D_1$  is to prevent the breakdown of gate cathode junction through  $D_2$  during negative half cycle.

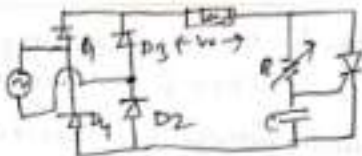
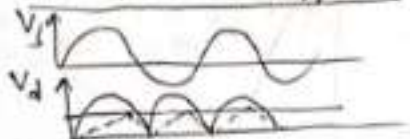


$$V_s > R I_{gt} + V_c$$

$$V_s > R I_{gt} + V_{gt} + V_d$$

$$V_d = \text{voltage drop across diode}$$

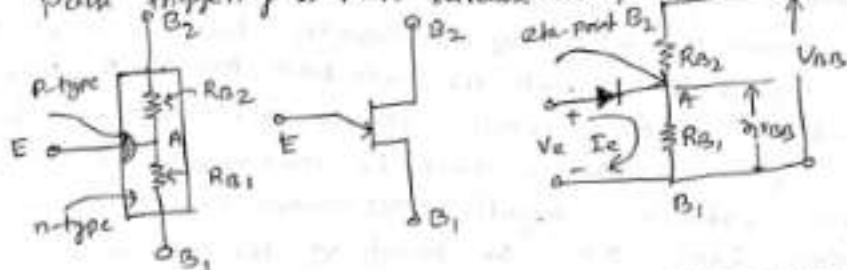
Rc full wave trigger cut:-



Unijunction Transistor (UJT) :-

\* pulse triggering is preferred as it offers several merits over R and R-C triggering. The power level in pulse triggering is low as the gate drive is discontinuous, pulse triggering is therefore more efficient.

\* A pulse with higher gate current are permissible, pulse triggering is more reliable and faster.



1 - A UJT is made up of n-type silicon base to which P-type emitter is embedded.

2 - It has three terminal, two base terminal B<sub>1</sub> and B<sub>2</sub> and one emitter terminal.

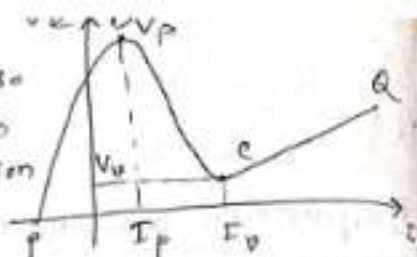
3 - The internal resistance R<sub>A1</sub> and R<sub>A2</sub> from the base B<sub>1</sub> and B<sub>2</sub>.

4 - When a voltage V<sub>AB</sub> is applied between two base terminals B<sub>1</sub> and B<sub>2</sub>, the potential of point A with respect to B<sub>1</sub>.

$$V_{A01} = \frac{V_{AB}}{R_{A1} + R_{A2}} \cdot R_{A1} = \frac{R_{A1}}{R_{A1} + R_{A2}} \cdot V_{AB} = \eta V_{AB}$$

$\eta = \frac{R_{A1}}{R_{A1} + R_{A2}}$  is called intrinsic stand-off ratio. Typical values of  $\eta$  are 0.51 to 0.82. For  $R_{A0} = R_{A1} + R_{A2}$  is the order of 5-10 K $\Omega$ .

Let  $V_E$  be the applied voltage between emitter E and base B, so that E is positive with respect to B. If  $V_E < \nabla V_{AB}$  the unijunction is reverse biased and emitter current is negative. When

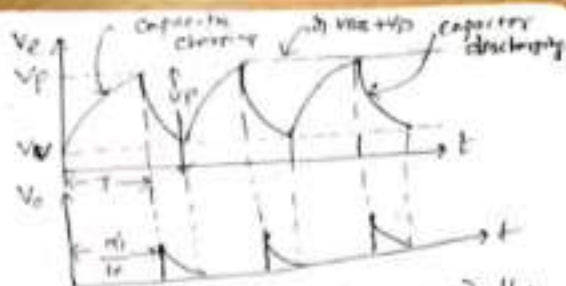
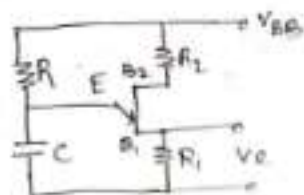


the emitter voltage  $V_E$  is equal to  $\nabla V_{AB} + V_D$  at point B,  $I_E$  is positive and E-B junction begins to conduct.  $V_D$  is the forward voltage drop of E-B junction. Point B is called "peak point" and corresponding emitter potential and current are denoted by  $V_P$  and  $I_P$  respectively. At point B, when  $V_E = \nabla V_{AB} + V_D$ , the emitter starts to inject holes into the lower base region 1. The resistance of E-B junction decreases, potential of emitter point falls and current  $I_E$  increases. Thus the device exhibits a negative resistance region which is shown line BC. At point C, the entire base region is saturated and resistance  $R_{B1}$  does not decrease any more. A further increase in  $I_E$  is accompanied by rise in voltage  $V_E$ . This line is CQ. Point C is called "valley point".

\* The negative resistance region between peak and valley point gives UJT switching characteristics for use in SCR triggering circuits.

**UJT oscillator triggering:** - The unijunction transistor is highly efficient switch. Its switching time is in the range of nanoseconds. So, UJT exhibits negative resistance characteristics. It can be used as relaxation oscillator. The circuit diagram of UJT works as oscillator mode. The external resistors  $R_1, R_2$  are small in comparison with the internal resistors  $R_{B1}, R_{B2}$  of UJT base.

When source voltage  $V_{AB}$  is applied, capacitor begins to charge through the capacitor resistor  $R$  by supply voltage  $V_{AB}$ , the voltage across it is exponential.



When emitter voltage reaches the peak point  $V_p$  ( $\eta V_{BB} + V_0$ ), the unijunction (unijunction) is breakdown. UJT conducts and capacitor  $C$  rapidly discharges through low resistance  $R_1$  with time constant  $\tau_2 = R_1 C$ . Here,  $\tau_2$  is lower than  $\tau_1$ . When emitter voltage decays to the valley point  $V_0$ , UJT turn-off. The time required for capacitor  $C$  to charge from initial voltage  $V_0$  to peak point  $V_p$ .

$$V_p = \eta V_{BB} + V_0 = V_0 + V_{BB} (1 - e^{-T/RC})$$

$$V_0 = V_e \quad \eta = (1 - e^{-T/RC})$$

$$T = \frac{1}{f} = RC \log_e \left( \frac{1}{1-\eta} \right)$$

$T$  is taken as output pulse duration.

$$\frac{V_{BB} \cdot R_1}{R_{BB} + R_1 + R_2} < \text{SCR trigger voltage } V_{gt}$$

$$R_{BB} = R_{B1} + R_{B2}$$

The emitter-diode forward characteristic vary with temperature, so that  $R_2$  is designed  $R_2 = \frac{I_0 T}{\eta V_{BB}}$

$$R_{max} = \frac{V_{BB} - V_p}{I_p} = \frac{V_{BB} - (\eta V_{BB} + V_0)}{I_p}$$

$$R_{min} = \frac{V_{BB} - V_0}{I_p}$$

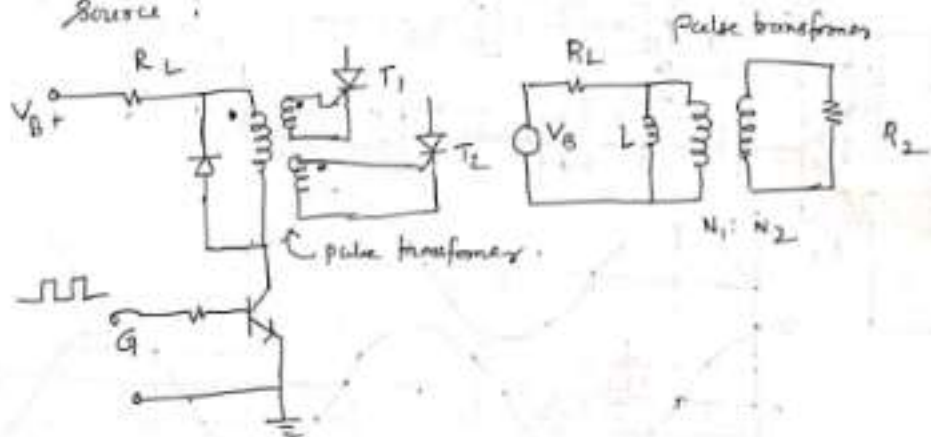
Problem A relaxation oscillator using an UJT, is to be designed for triggering an SCR. The UJT has following data

$\eta = 0.72$ ,  $I_p = 0.6 \text{ mA}$ ,  $V_p = 18.0 \text{ V}$ ,  $V_0 = 1.0 \text{ V}$ ,  $I_0 = 2.5 \text{ mA}$ ,  $R_{BB} = 5 \text{ k}\Omega$ . Normal leakage current with emitter open  $4.2 \text{ mA}$ . The firing frequency is  $2 \text{ kHz}$ . For  $C = 0.04 \text{ }\mu\text{F}$  compute the value of  $R_1$  and  $R_2$ .

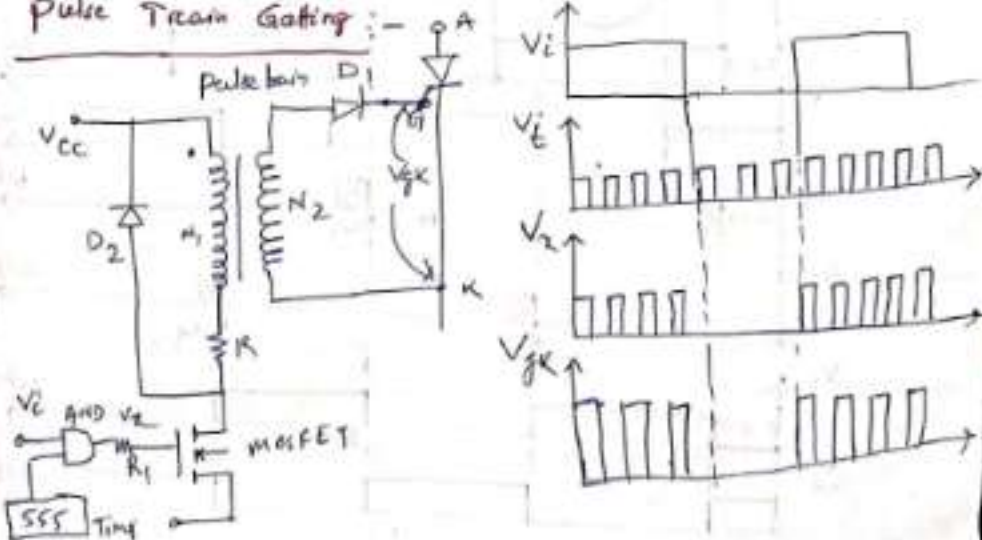


Pulse transformer :- Pulse transformers are used quite often in firing circuits for SCR and GTOs. This transformer has usually two secondaries. The turn ratio from primary to two secondaries is 2:1:1 or 1:1:1. These transformers are designed to have low winding resistance, low leakage reactance and low inter winding capacitance. The advantage of using pulse transformer in triggering semiconductor devices

- (i) the isolation of low voltage gate circuit from test voltage and circuit.
- (ii) the trigger of two or more device from the same trigger source.



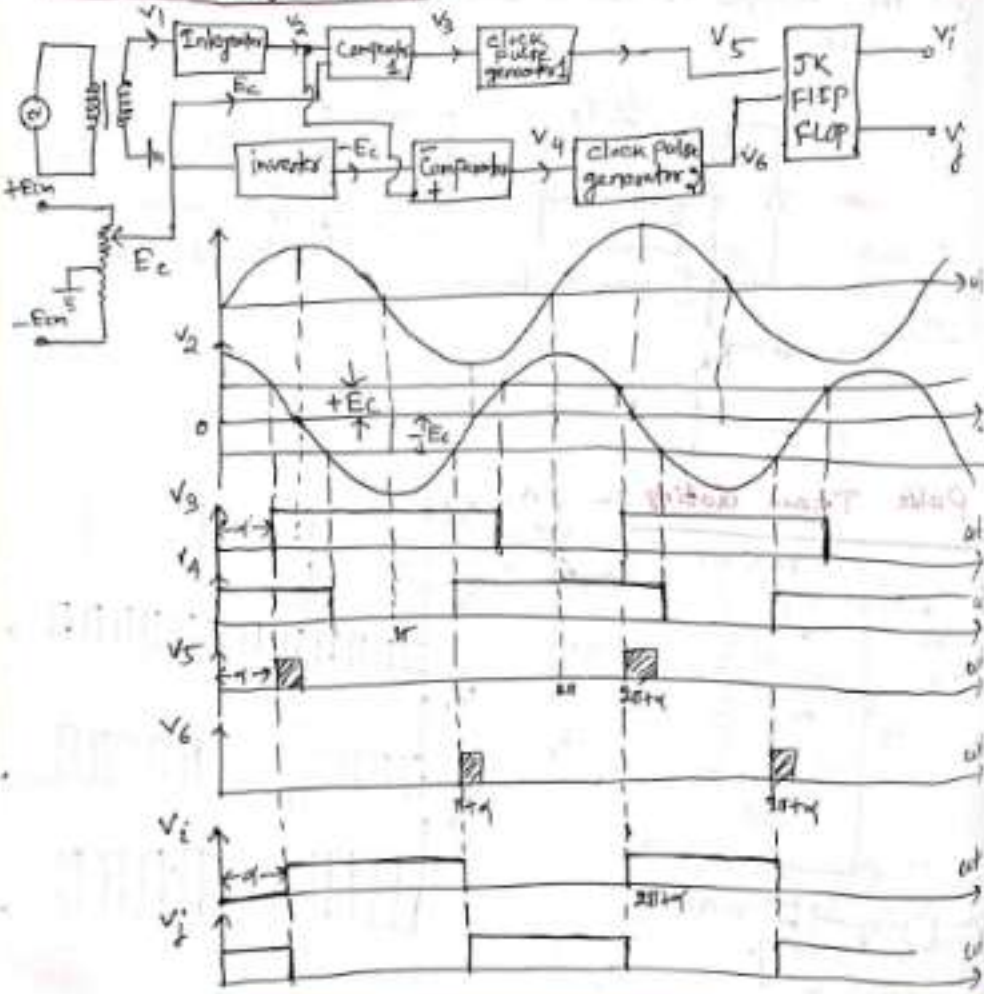
Pulse Train Gating :-



1. continuous gating suffers from disadvantages like increase in thyristor losses and distortion of output pulse due to saturation of pulse transformer by continuous pulse.

2. In order to overcome these shortcomings of continuous gating signals, a train of first pulse is used to turn on a thyristor. A pulse train of gating signal is also called high frequency carrier gating. A pulse train can be generated by modulating the pulse width at a high frequency (10 to 30 kHz)

Cosine firing scheme:-



1. The synchronizing transformer steps down the supply voltage to an appropriate level.
2. The 90 voltage  $V_1$  is integrated to get cosine wave  $V_2$ .
3. The d.c control voltage  $E_c$  varies from maximum positive  $E_{cm}$  to maximum negative  $E_{cm}$  so that firing angle can be varied from 0 to  $180^\circ$ .
4. The cosine wave  $V_2$  is compared in comparator 1 and 2 with  $E_c$  and  $-E_c$ .
5. The comparator 1 and 2 give output pulse  $V_3$  and  $V_4$  respectively.
6. firing angle is governed by the interaction of  $V_2$  and  $E_c$ . When  $E_c$  is maximum, firing angle is zero. This firing angle  $\alpha$  in terms of  $V_{2m}$  and  $E_c$  can be expressed as
 
$$V_{2m} \cos \alpha = E_c \quad \therefore \alpha = \cos^{-1} \left( \frac{E_c}{V_{2m}} \right)$$
7. The signal  $V_3, V_4$  obtained from comparators are fed to clock pulse generator 1, 2 to get clock pulse  $V_5, V_6$ . These signals  $V_5, V_6$  energize a JK flip flop to generate output signals  $V_i, V_f$ .

$$V_o = \frac{2V_m}{\pi} \cos \alpha$$

$$V_o = \frac{2V_m}{\pi} \cos \left[ \cos^{-1} \frac{E_c}{V_{2m}} \right] = \left[ \frac{2V_m}{\pi} \cdot \frac{1}{V_{2m}} \right] E_c$$

$$V_o = K E_c$$

Cosine firing scheme provides a linear transfer characteristic between the average output voltage  $V_o$  and control voltage  $E_c$ . This scheme, on account of its linear transfer characteristic improve closed loop response of the converter system. This features has made the cosine firing scheme quite popular in industrial application.

## Series and parallel operations

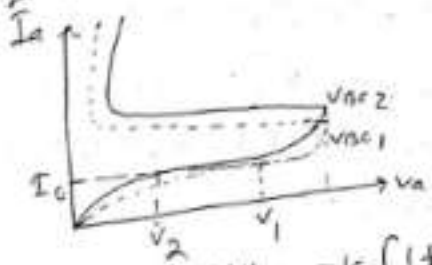
1. SCRs are connected in series in order to meet the h.v demand and in parallel for fulfilling the high current demand. For series or parallel connected SCR, it should be ensured that each SCR rating is fully utilized and system operation is satisfactory.
2. String efficiency is a term that is used for measuring the degree of utilization of SCR in a string.

$$\text{String efficiency} = \frac{\text{Actual voltage/current rating of the whole string}}{\left[ \text{individual voltage/current rating of one SCR} \right] \left[ \text{Number of SCRs in the string} \right]}$$

3. This ratio is less than 1. For obtaining highest possible string efficiency, the SCR connected in series/parallel string must have identical v-I characteristics. As SCRs have same rating and specification do not have identical characteristics, unequal voltage/current sharing is bound to occur for all SCRs in a string. So string efficiency is never equal to 1.
4. In case one extra unit is added to series/parallel string, the voltage and current shared by each device would become lower than its normal rating. The use of this extra unit will certainly improve the reliability of the string though at an increased cost.
5. A measure of the reliability of string is given by a factor called derating factor DRF  
$$\text{DRF} = 1 - \text{string efficiency}$$
6. If the value of recommended DRF is more, no. of device used in series/parallel string will be more.

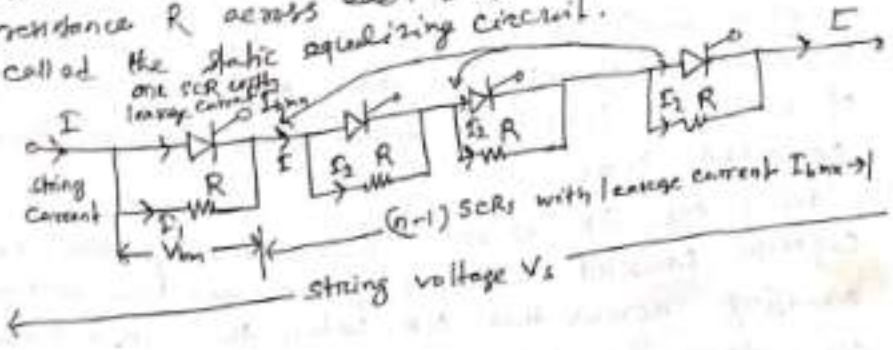
## Series operation:

1. When system voltage is more than the voltage rating of single thyristor, SCRs are connected in series in a string.
2. Due to inherent variations in their characteristics the voltage shared by each SCR may not be equal.
3. For some leakage current  $I_0$ ,  $V_2$  is less than  $V_1$ .



The string efficiency is 
$$\frac{V_1 + V_2}{2V_1} = \frac{1}{2} \left( 1 + \frac{V_2}{V_1} \right)$$

- \* Though SCRs have identical rating, voltage shared by each is not the same and string efficiency is less than 1.
- \* A uniform voltage distribution in steady state can be achieved by connecting a suitable resistance across each SCR such that each parallel combination has the same resistance. A very practical way of establishing uniform voltage distribution during steady state working of series connected SCRs is to connect the same value of shunt resistance  $R$  across each SCR. The shunt resistance  $R$  is called the static equalizing circuit.



considers  $n$  thyristors connected in series. Let SCR1 has minimum leakage current  $I_{bmn}$  and each of the remaining  $(n-1)$  SCRs have the same leakage current  $I_{bmx} > I_{bmn}$ . SCR1 has lower leakage current, it will block voltage  $V_{bm}$  which is more than that shared by each of the other  $(n-1)$  SCRs.

$$I_1 = I - I_{bmn} \quad I_2 = I - I_{bmx}$$

$V_{bm} = I_1 R$ , voltage across  $(n-1)$  SCRs  $= (n-1) I_2 R$

$$V_s = I_1 R + (n-1) I_2 R = V_{bm} + (n-1)(I - I_{bmx}) R$$

$$= V_{bm} + (n-1) R [I_1 - (I_{bmx} - I_{bmn})]$$

$$= V_{bm} + (n-1) R I_1 - (n-1) R \cdot \Delta I_b$$

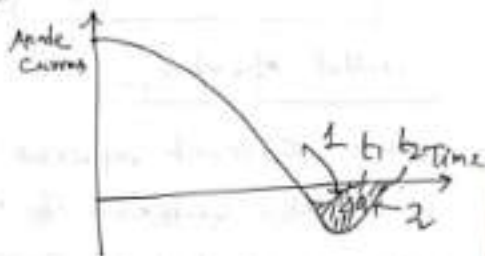
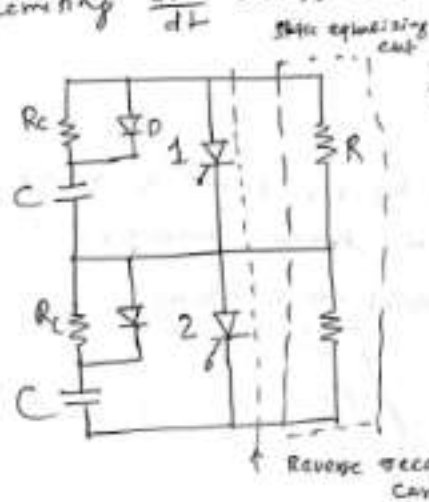
$$\Delta I_b = I_{bmx} - I_{bmn}$$

$$V_s = n V_{bm} - (n-1) R \cdot \Delta I_b$$

$$R = \frac{n V_{bm} - V_s}{(n-1) \Delta I_b}$$

- \* Static voltage equalization cannot maintain equal voltage distribution under transient condition.
- \* During reverse bias condition, voltage distribution of each SCR will be different due to their different self capacitance. As reverse-biased junctions are likely to have different capacitance, called self capacitance, the voltage distribution during turn-on and turn-off period would be unequal. During turn on and turn off period the resultant shunt capacitance and self capacitance of each SCR tend to be equal for each of the series connected SCRs.
- \* When any SCR is in the forward blocking state, the capacitors connected across it get charged to a voltage existing across that SCR. When this SCR is turned on, capacitor discharges heavy current through it.

SCR. For limiting the discharge current, damping resistor  $R_c$  is used in series with capacitor  $C$ . The function of resistance  $R_c$  is damps out the high frequency oscillation, combination of  $R_c$  and  $C$  called the dynamic equalizing circuit. A diode  $D$  is placed  $R_c$ . When forward voltage appears, diode bypass  $R_c$  during charging time of the capacitor  $C$ . This makes the capacitor more effective in voltage equalization and limiting  $\frac{dv}{dt}$  across SCR.



SCR<sub>1</sub> is assumed to have short reverse recovery time as compared to SCR<sub>2</sub>. Shaded area  $\Delta Q$  proportional to the product of current and time. SCR<sub>1</sub> recovers first, it is therefore goes into blocking state and does not allow the passage of excess charge  $\Delta Q$  left on SCR<sub>2</sub>. The thyristor with the least reverse recovery time will share the highest transient voltage say  $V_m$ . As voltage difference to which the two thyristors are charged during reverse recovery time is  $\Delta Q/C$ , the transient voltage shared by slow thyristor 2 must be  $V_m - \frac{\Delta Q}{C}$

$$V_1 = V_m$$

$$V_2 = V_m - \frac{\Delta Q}{C}$$

$$V_c = V_1 + V_2 = V_m + V_m - \frac{\Delta Q}{C}$$

$$V_{tm} = \frac{1}{2} \left( V_s + \frac{4B}{C} \right)$$

$$V_2 = V_{tm} - \frac{4B}{C} = \frac{1}{2} \left( V_s - \frac{4B}{C} \right)$$

$$V_s = V_1 + (n-1)V_2$$

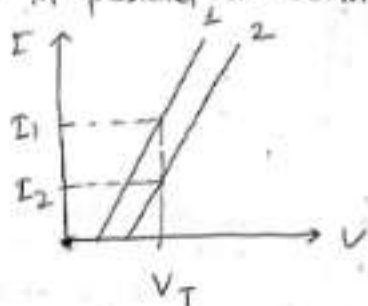
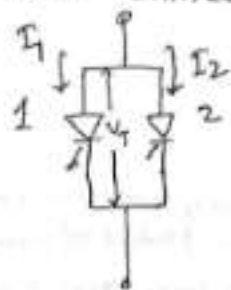
$$= V_{tm} + (n-1) \left( V_{tm} - \frac{4B}{C} \right)$$

$$V_{tm} = \frac{1}{n} \left[ V_s + \frac{(n-1)4B}{C} \right]$$

$$C = \frac{(n-1)4B}{nV_{tm} - V_s}$$

Parallel operation:-

When current required by the load is more than rated current of a single thyristor, SCRs are connected in parallel in a string.

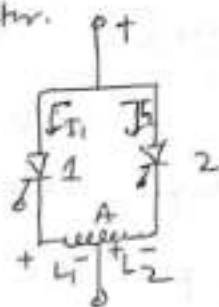


For equal sharing of current,  $V-I$  characteristics of SCRs during forward conduction must be identical. For parallel operation of SCRs,  $V_T$  across them must be equal. For same voltage drop  $V_T$ , SCR1 shares a rated current  $I_1$  whereas SCR2 carries current  $I_2$  much less than rated current  $I_1$ . The total current carried by  $I_1 + I_2$ .

The string efficiency

$$\frac{I_1 + I_2}{2I_1} = \frac{1}{2} \left( 1 + \frac{I_2}{I_1} \right)$$

A unequal current distribution in a parallel unit is also caused by the inductive effect of current carrying conductor.



Problem :- A string of four series connected thyristors is provided with static and dynamic equalizing circuit. The string has to withstand on off state voltage of 10kV. The static equalizing resistance is  $25000\Omega$  and dynamic equalizing circuit has  $R_c = 40\Omega$  and  $C = 0.09\mu F$ .

The leakage current of four thyristors are 21 mA, 25 mA, 18 mA and 16 mA respectively. Determine the voltage across each SCR in the off state and discharge current of each capacitor at the time of turn on.

Sol<sup>n</sup> :- Let  $I$  be the string current in the off state. Then current through static equalizing resistance  $R$  of  $25000\Omega$  is  $(I - \text{leakage current})$ , current

through each SCR is its own current.

$$\text{Voltage across SCR}_1 = (I - 0.021) \times 25000$$

$$\text{Voltage across SCR}_2 = (I - 0.025) \times 25000$$

$$\text{Voltage across SCR}_3 = (I - 0.018) \times 25000$$

$$\text{Voltage across SCR}_4 = (I - 0.016) \times 25000$$

$$25000(4I - 0.08) = V_1 + V_2 + V_3 + V_4 = 100000$$

$$I = 0.12 \text{ A}$$

$$\text{Voltage across SCR}_1 = (0.12 - 0.021) \times 25000 = 2475 \text{ V}$$

$$V_2 = 2375 \text{ V} \quad V_3 = 2550 \text{ V} \quad V_4 = 2600 \text{ V}$$

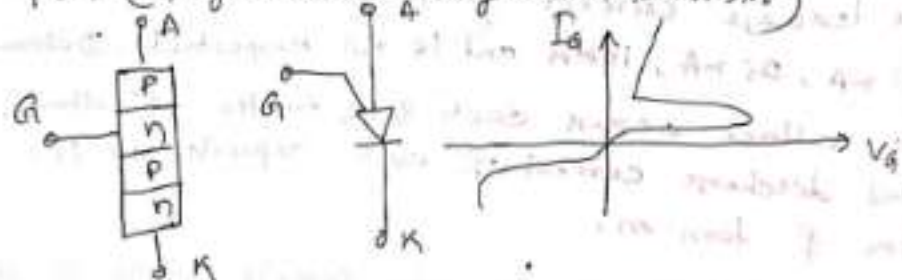
Discharge current through SCR<sub>1</sub> at the time of turn on

$$= \frac{V_1}{R_c} = \frac{2475}{40} = 61.875 \text{ A}$$

Similarly discharge current through the thyristors 2, 3 and 4 respectively 59.375 A, 63.75 A and 65 A.

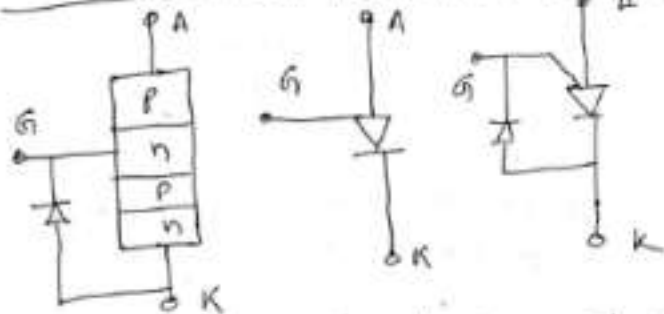
Thyristor family members:

PUT (programmable unijunction transistor)



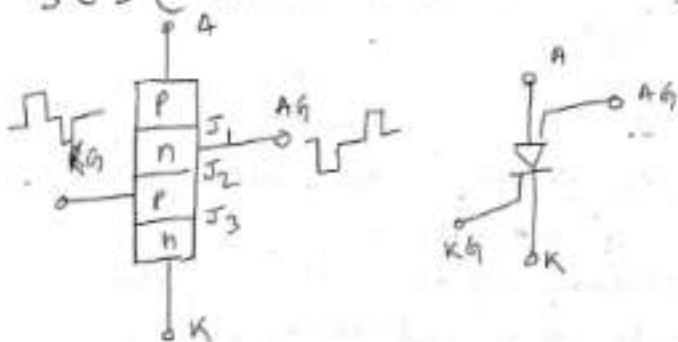
It is a pnpn device. The major difference is that gate is connected to n-type material near the anode.

## SUS (Silicon unilaterial switch)



A SUS is similar to PUT with an inbuilt low voltage avalanche diode between gate and cathode.

## SCS (Silicon controlled Switch)



SCS is a tetrode. It has two gates, one is anode gate like a PUT and another cathode gate (KG) like an SCR.

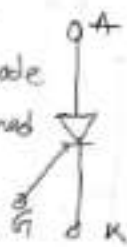
## Light activated Thyristors :-

The diagram shows a Light Activated Silicon Controlled Rectifier (LASCR). It has a vertical stack of P, n, P, n layers. The top P layer is the Anode (A), the bottom n layer is the Cathode (K), and the middle P layer is the Cathode Gate (KG). A pulse waveform is shown at the KG terminal. Light rays are shown entering from the top, hitting the Anode (A) terminal, and being directed towards the junction between the top P and n layers.

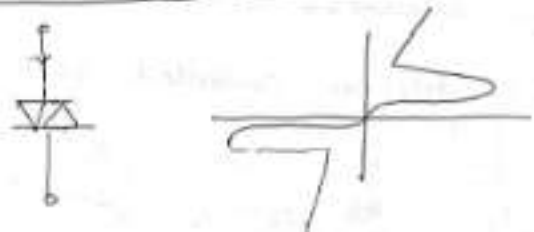
LASCR are turned on by throwing a pulse of light on the silicon wafer of thyristors. The pulse of appropriate wavelength is guided by optical fibres to the special sensitive area of the wafer.

## Static Induction Thyristor (SITH)

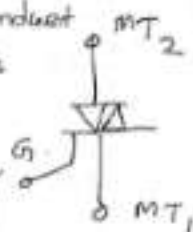
SITH is turned on by applying short positive pulse between gate and cathode like an ordinary thyristor. It is turned off by the application of short negative pulse of large current between gate and cathode.



## Diac (Bidirectional Thyristor Diode)



The Triac :- An triac can conduct ~~forward~~ in both directions. A triac is thus a bidirectional thyristor with three terminals. It is used extensively for the control of ac circuits.



## Asymmetrical Thyristor (ASCR)

An asymmetrical thyristor or ASCR is specially fabricated to have limited reverse voltage capability. So this permits a reduction in turn on time, turn-off time and on-state voltage drop in ASCR.

## Reverse conducting Thyristor (RCT)

A reverse conducting thyristor is a special case asymmetrical thyristor with a monolithic

integrated antiparallel diode on the same silicon chip. This construction reduces to zero the reverse blocking capability of RCT. It reduces the heat sink size and leads to compactness of the converter.

### Gate turn off (GTO) Thyristor

A gate turn-off thyristor, a P-N-P-N device can be turned on by positive gate current and turned off by negative gate pulse of appropriate amplitude.

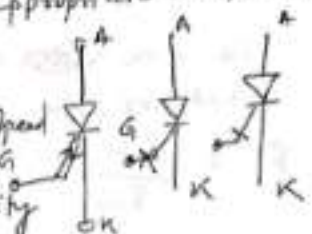
GTO has certain advantages:

- (i) GTO has faster switching speed
- (ii) Its surge current capability is comparable with an SCR.
- (iii) It has more  $di/dt$  rating at turn-on.
- (iv) GTO circuit configuration has lower size and weight as compared to SCR circuit unit.
- (v) GTO has higher efficiency
- (vi) GTO unit has reduced acoustical and electromagnetic noise due to elimination of commutation chokes.

Disadvantages: - (i) magnitude of latching and holding

current is more in a GTO

- (ii) on state voltage drop and associated loss is more in a GTO
- (iii) Gate drive circuit losses are more.



- (iv) Gate drive circuit losses are more.
- (v) It's reverse voltage blocking capability is less than its forward-voltage blocking capability.

### Thyristor rating

$I_{AV}$  = forward on state voltage across a thyristor  $I_{AV}$

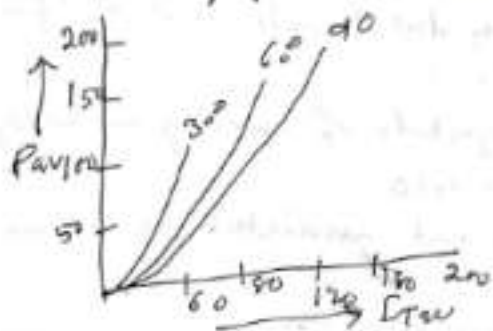
$$P_{AV} = \frac{1}{T} \int (instantaneous \text{ voltage across SCR}) (instantaneous \text{ current through SCR}) dt$$

Where  $T$  = periodic time of the anode current waveform

- \* The rms value of current for an SCR is constant, whatever the conduction angle.

$$FF = \frac{I_{RMS}}{I_{AV}} \quad \therefore I_{AV} = \frac{I_{RMS}}{FF}$$

- \* For same conduction angle, the form factor of sine wave is higher than rectangular wave. The average current for sine wave will be lower than for rectangular wave for the same dc. The derating of the SCR is therefore more for sine wave than for square or rectangular wave.

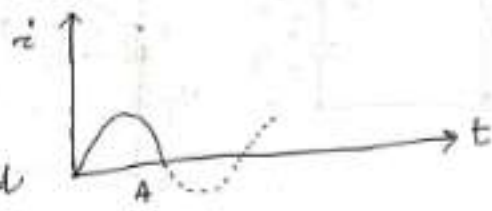
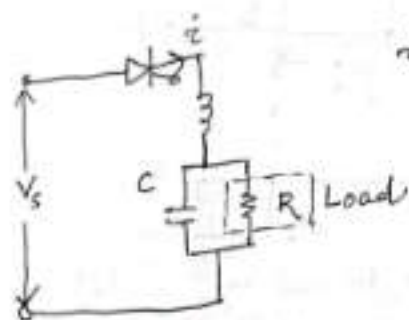
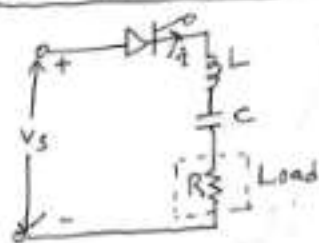


## **MODULE- II**

## Thyristor commutation Techniques

The purpose of commutation means how to turn off a thyristor means bringing the device from forward conduction state to forward-blocking state. Commutation is defined as the process of turning-off a thyristor. Once thyristor starts conducting, gate loses control of over the device, so external means may have to be adopted to commutate the thyristor. Several commutation techniques have been developed with side objectives of reducing their turn-off time.

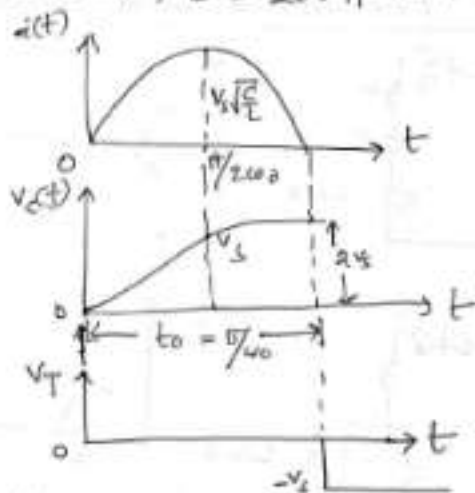
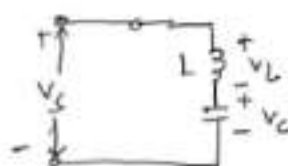
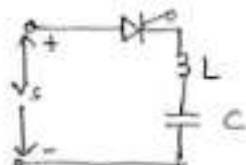
Class A commutation: Load commutation:-



For obtaining load commutation of thyristor, the commutating components  $L$  and  $C$  are connected. For low value of  $R$ ,  $L$  and  $C$  are connected in series. For high value of  $R$ , Load  $R$  is connected parallel across  $C$ . The overall circuit behaves as under-damped. It is obtained, current  $i$  first rises to maximum value and begins to fall. When current

decays to zero and tends to reverse, the thyristor is turned off at instant A. Load or class A commutation is prevalent in thyristor circuits supplied from dc source. Load commutation is possible in dc circuit and not in ac circuit. Class B or load commutation is also called resonant commutation or self commutation.

Example 1. The circuit shown in fig is initially relaxed. The thyristor T is turned on at  $t=0$ . Determine (a) conduction time of thyristor (b) voltage across thyristor and capacitor after SCR is turned off. Calculate the values for  $L = 5 \text{ mH}$ ,  $C = 20 \text{ } \mu\text{F}$  and  $V_s = 200 \text{ V}$ .



Sol<sup>n</sup>

When thyristor is turned on, it behaves like a diode. Therefore, with SCR on, the device acts like a closed switch. KVL for this circuit

$$L \frac{di}{dt} + \frac{1}{C} \int i dt = V_s$$

$$\textcircled{a} \quad i(t) = V_s \sqrt{\frac{C}{L}} \sin \omega_0 t$$

$\omega_0 = \frac{1}{\sqrt{LC}}$  is called resonant frequency of the circuit.

capacitor voltage  $V_c(t) = V_s(1 - \cos \omega t)$

when  $t = \pi/\omega$ ,  $V_c(t) = +2V_s$ . After  $\pi/\omega$  sec or  $\pi\sqrt{LC}$  sec the thyristor is closed at  $t=0$ , the charging current becomes zero. The thyristor is turned off.

$t_o$  = conduction time of the thyristor =  $\pi\sqrt{LC}$

The voltage across the thyristor  $V_T = -2V_s + V_c = -V_s$

Resonant frequency of the circuit  $\omega_o = \frac{1}{\sqrt{LC}}$

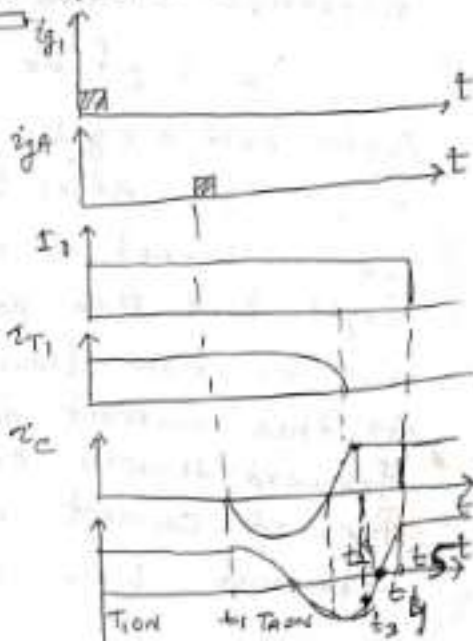
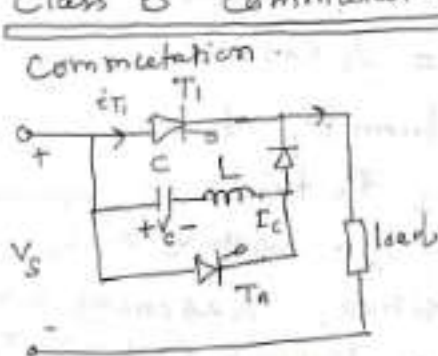
$$= \frac{10^4}{\sqrt{10}} = 3162.27 \text{ rad/sec.}$$

conduction time of thyristor  $t_o = \pi/\omega_o = \frac{\pi\sqrt{LC}}{10^4}$

$$9.9346 \times 10^{-3} \text{ s} = 0.99346 \text{ ms}$$

voltage across thyristor after it is turned off  
 $= -V_s = -200 \text{ V}$ .

### Class B commutation: Resonant pulse



Initially the capacitor  $C$  charges to <sup>from</sup> source voltage  $V_s$  with left positive. Main thyristor  $T_1$  and auxiliary thyristor  $T_A$  are off. Positive direction of capacitor voltage  $V_c$  and capacitor current marked. Load current is assumed to be constant.

At time  $t_1$ ,  $V_c = V_s$ ,  $i_c = 0$ ,  $i_o = I_o$ . For turning off the main thyristor  $T_1$ , auxiliary thyristor  $T_A$  is gated on at  $t = t_1$ . With  $T_A$  is on, a resonant current  $i_c$  begins to flow from  $C \rightarrow T_A \rightarrow L \rightarrow C$ . At  $t_1$ , the resonant current  $i_c = -V_s \sqrt{\frac{C}{L}} \sin \omega t$   
 $= -I_p \sin \omega t$ .

Minus sign before  $I_p \sin \omega t$  is due to the fact that this current flows opposite to the reference positive direction chosen.

$$V_c = \frac{1}{C} \int i_c dt = V_s \cos \omega t.$$

After half a cycle from  $t_1$ ,  $i_c = 0$ ,  $V_c = -V_s$ ,  $i_{T_1} = I_o$ . After  $t_2$   $i_c$  tends to reverse.  $T_A$  is turned off at  $t_2$ . With  $V_c = -V_s$  right hand plate positive. Resonant current  $i_c$  is now flowing through  $C \rightarrow L \rightarrow D \rightarrow T_1$ . As this current  $i_c$  grows opposite to forward thyristor current of  $T_1$ , net forward current  $i_{T_1} = I_o - i_c$  begins to decrease. When  $-i_c$  becomes equal

to  $I_0$ , forward current in  $T_1$ ,  $I_0 - I_0 = 0$ .  
The device is turned off. For reliable

commutation, peak resonant current  $I_p$  must be greater than load current  $I_0$ .  
As thyristor is commutated by the gradual build up of resonant current in the reverse direction this method of commutation is called current commutation, class B commutation, resonant commutation.

After  $T_1$  is turned off at  $t_3$ , constant current  $I_0$  flows from  $V_s$  to load through C, L and D. Capacitor begins to charge from  $-V_{ab}$  to zero and then to  $V_s$  at  $t_5$ .

Main thyristor  $T_1$  is turned off when

$$V_s \sqrt{\frac{C}{L}} \sin \omega_0 (t_3 - t_2) = I_0$$

$$\omega_0 (t_3 - t_2) = \sin^{-1} \left( \frac{I_0}{I_p} \right)$$

$$I_p = V_s \sqrt{\frac{C}{L}} \text{ Peak resonant current.}$$

Circuit turn-off time for main thyristor

$$t_c = t_4 - t_3 = C \frac{V_{ab}}{I_0}$$

Voltage across the main thyristor when it gets commutated

$$V_{ab} = V_s \cos \omega_0 (t_3 - t_2)$$

Example :- In a resonant pulse commutation (or class B commutation) has  $C = 20 \mu\text{F}$  and  $L = 5 \text{ mH}$ . Initial voltage across capacitor is  $V_s = 230 \text{ V}$ . For constant load current of  $30 \text{ A}$ .

- Conduction time for the auxiliary thyristor
- voltage across the main thyristor when it gets commutated
- Circuit turn-off time for main thyristor

Solution :- Peak value of resonant current

$$I_p = V_s \sqrt{\frac{C}{L}} = 230 \sqrt{\frac{20}{5}} = 460 \text{ A}$$

resonant frequency  $\omega_0 = \frac{1}{\sqrt{LC}} = \frac{10^6}{\sqrt{100}} = 0.1 \times 10^6 \text{ rad/s}$

- Conduction time for auxiliary thyristor  

$$= \frac{\pi}{\omega_0} = \frac{\pi}{0.1 \times 10^6} = 31.4159 \text{ } \mu\text{s}$$

- $\omega_0 (t_3 - t_2) = \sin^{-1}\left(\frac{300}{460}\right) = 40.706^\circ$  or  $0.71045 \text{ rad}$   
 Voltage across main thyristor when it gets turned off  

$$V_{ab} = V_s \cos \omega_0 (t_3 - t_2) = 230 \cos(40.706^\circ)$$

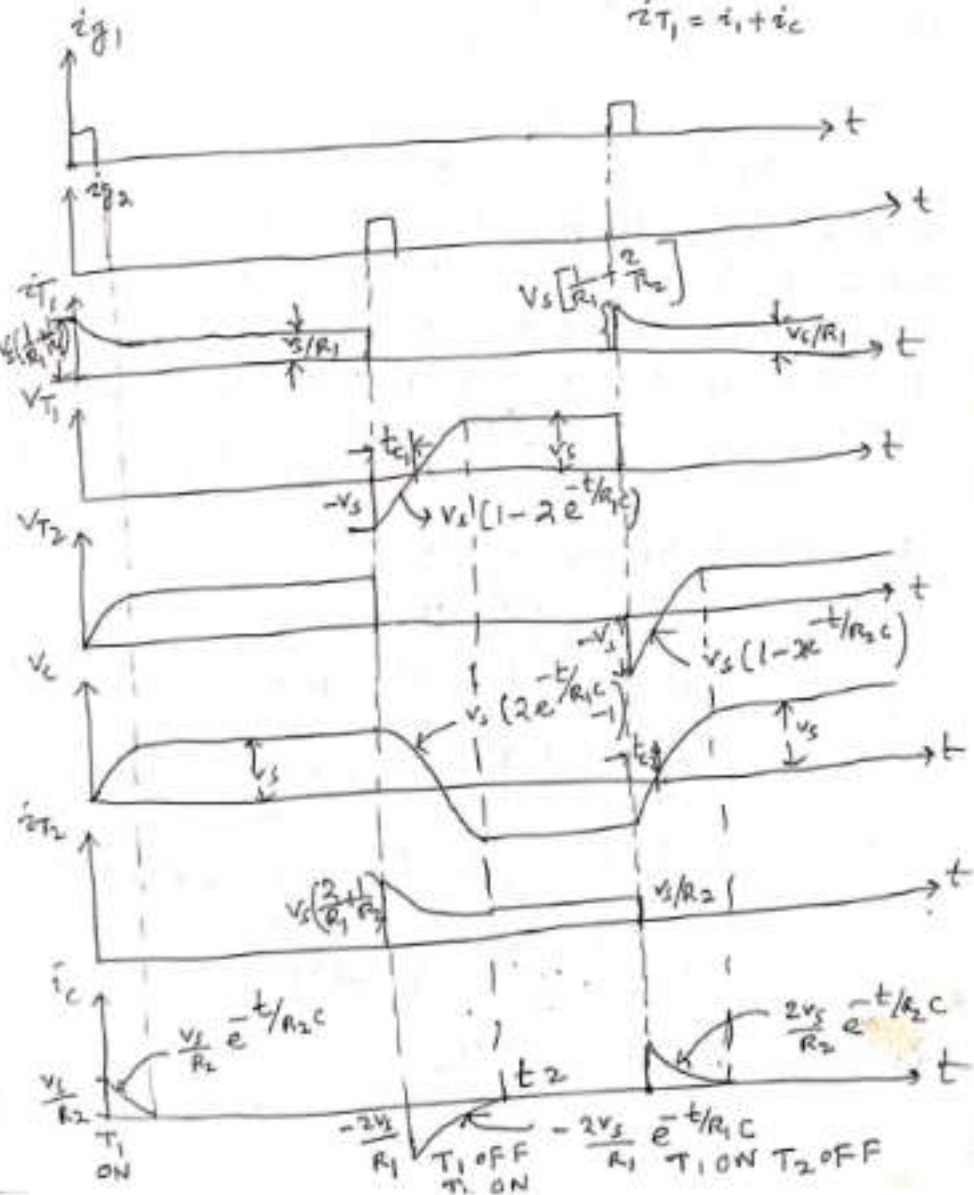
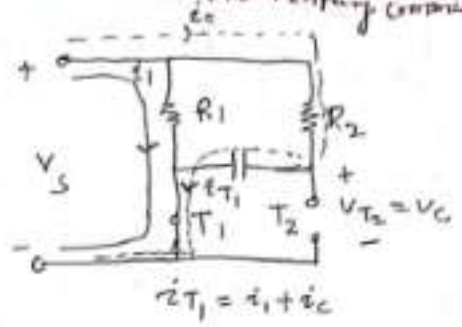
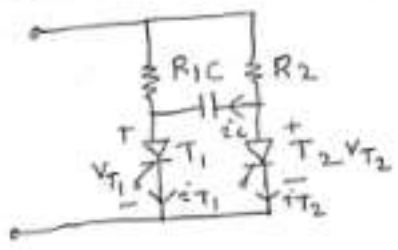
$$= 174.355 \text{ V}$$

- circuit turn-off time for main thyristor  

$$t_c = t_4 - t_3 = C \frac{V_{ab}}{I_a} = 20 \times 10^{-6} \frac{174.355}{30}$$

$$= 11.624 \text{ } \mu\text{s}$$

class c commutation: - Complementary commutation



In this type of commutation, one thyristor is commutated by another thyristor. SCR  $T_1$  commutates  $T_2$  and subsequently firing of SCR  $T_2$  would turn-off  $T_1$ . When  $T_1$  is turned on at  $t=0$  current through  $R_1$  is  $i_{T_1}$  and through  $R_2$  is  $i_c = \frac{V_s}{R_2}$  so  $i_{T_1}$  is  $i_1 + i_c = V_s \left( \frac{1}{R_1} + \frac{1}{R_2} \right)$ . Capacitor is charging through  $R_2$ .  
 The charging current through  $V_s - C - R_2$ .

$$i_c(t) = \frac{V_s}{R_2} e^{-t/R_2 C}$$

$$V_c(t) = V_s \left( 1 - e^{-t/R_2 C} \right)$$

voltage across thyristor  $T_2$  is  $V_{T_2} = V_c(t)$   
 When  $T_2$  is turned on at  $t_1$ ,  $T_1$  is turned off because capacitor voltage  $V_c$  applies a reverse potential  $V_s$  across SCR  $T_1$ . At  $t_1$ ,  $V_{T_2} = 0$   
 $V_{T_1} = -V_s$   $i_c = -\frac{2V_s}{R_1}$   $i_{T_2} = V_s \left( \frac{2}{R_1} + \frac{1}{R_2} \right)$

for circuit  $V_s - R_1 - C - T_2$

$$R_1 i_c + \frac{1}{C} \int i_c dt = V_s$$

$$R_1 I_c(s) + \frac{1}{C} \left[ \frac{I_c(s)}{s} + \frac{q_0(s)}{s} \right] = \frac{V_s}{s}$$

$$R_1 I_c(s) + \frac{1}{C} \left[ \frac{-I_c(s)}{s} - \frac{C V_s}{s} \right] = \frac{V_s}{s}$$

$$R_1 I_c(s) + \frac{1}{C} \frac{I_c(s)}{s} = \frac{V_s}{s} + \frac{2V_s}{s}$$

$$I_c(s) \left[ R_1 + \frac{1}{C s} \right] = \frac{2V_s}{s}$$

$$I_c(s) = \frac{2V_s}{s \left( R_1 + \frac{1}{C s} \right)} = \frac{2V_s C s}{s(R_1 C s + 1)}$$

$$F_c(s) = \frac{2V_c R / R_1 C}{s + \frac{1}{R_1 C}} = \frac{2V_s}{R_1} \left( \frac{1}{s + R_1 C} \right)$$

$$i_c(t) = \frac{2V_s}{R_1} e^{-t/R_1 C}$$

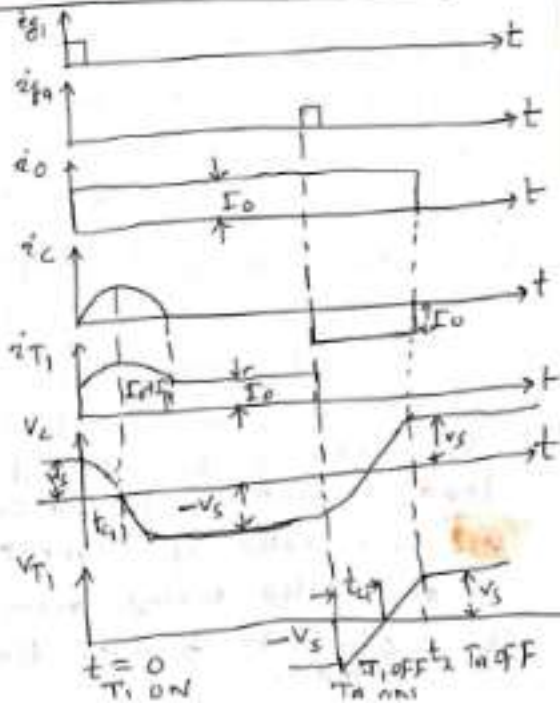
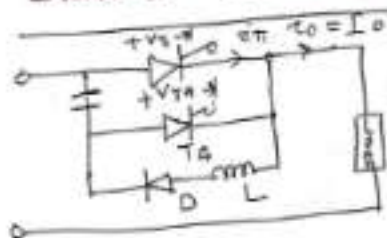
voltage across capacitor  $V_c(t) = \left[ \frac{1}{C} \int_0^t i_c dt + V_s \right]$

$$= \frac{1}{C} \int \left[ -\frac{2V_s}{R_1} e^{-t/R_1 C} + V_s \right] = V_s \left[ 2 e^{-t/R_1 C} - 1 \right]$$

Current  $i_{T_2}$  falls from its value  $V_s \left[ \frac{2}{R_1} + \frac{1}{R_2} \right]$  to  $V_s/R_2$  with time constant  $R_1 C$

With the turn on of  $T_2$  at  $t_1$ , capacitor voltage  $V_s$  suddenly appears as reverse bias across  $T_1$  to turn it off. Similarly at  $t_2$  capacitor voltage  $V_s$  applies reverse bias across  $T_2$  to turn it off. class C commutation is also called complementary impulse commutation.

class D Commutation. (Impulse commutation)



Initially main thyristor  $T_1$  and auxiliary thyristor  $T_2$  are off and capacitor is assumed charged to voltage  $V_s$  with upper plate positive.

1. When  $T_1$  is turned on at  $t=0$ , load current  $I_o$  begins to flow which is constant load current.  $T_1$  is on at  $t=0$ . An oscillatory circuit consisting of  $C$ ,  $T_1$ ,  $L$  and  $D$  is formed, whose the capacitor current is given by

$$i_c = V_s \sqrt{\frac{C}{L}} \sin \omega t = I_p \sin \omega t.$$

between  $0 < t < \omega \pi / \omega_0$ ,  $i_{T_1} = I_o + I_p \sin \omega t$ . At  $\omega t = \pi$   $i_c = 0$ ,  $i_{T_1} = I_o$   $V_c = -V_s$ .

2. At  $t_1$ ,  $T_2$  is turned on, capacitor with  $V_c$  applies a reverse voltage across main thyristor  $T_1$ , so that  $V_{T_1} = -V_s$ . At  $t_2$  SCR  $T_1$  is turned off. Load current flows through  $C-T_2$ . Capacitor gets charged to  $-V_c$  to  $V_s$  with constant load current  $I_o$ . The charges is, therefore, linear from  $+V_c$  to  $-V_s$  when  $V_c = V_s$   $i_c = 0$  at  $t_2$ ,  $T_2$  is turned off.

With the firing of thyristor  $T_2$ , a reverse voltage  $V_c$  is suddenly applied across  $T_1$ . The method of commutation is therefore voltage commutation.

Example 5.4 . For class D commutation. For this case  $V_s = 230V$   $L = 20 \mu H$  and  $C = 40 \mu F$ . For constant load current of  $120A$ . Calculate

- (a) peak value of current through capacitance and also through main & auxiliary thyristor.  
 (b) circuit turn off time for main and auxiliary thyristor.

Soln

$$i_c(t) = V_s \sqrt{\frac{C}{L}} \sin \omega t$$

∴ peak value of current through main thyristor

$$T_1 = I_p + I_0$$

$$I_p = V_s \sqrt{\frac{C}{L}} = 230 \sqrt{\frac{40}{20}} = 325.22 \text{ A}$$

peak value of current through main thyristor

$$T_1 = I_p + I_0 = 325.22 + 120 = 445.22 \text{ A}$$

peak value of current through auxiliary thyristor

$$T_A = I_0 = 120 \text{ A}$$

(b) circuit turn-off time for main thyristor

$$T_1 \therefore t_c = \frac{C V_s}{I_0}$$

$$t_c = \frac{C V_s}{I_0} = \frac{40 \times 10^{-6} \times 230}{120} = 76.67 \mu\text{sec}$$

Circuit turn-off time  $t_c$  for  $T_A = \pi / 2\omega_0$

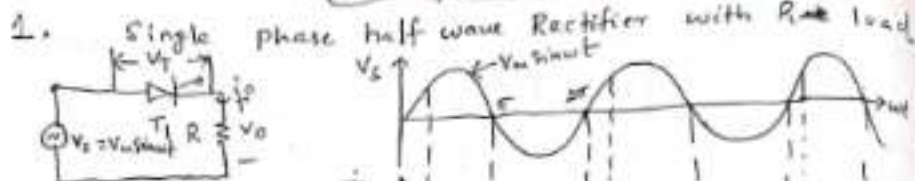
$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{10^6}{\sqrt{20 \times 40}} = \frac{10^6}{\sqrt{800}}$$

$$t_{c1} = \frac{\pi}{2\omega_0} = \frac{\pi \sqrt{800}}{2 \times 10^6} = 44.42 \mu\text{sec}$$

Class E Commutation

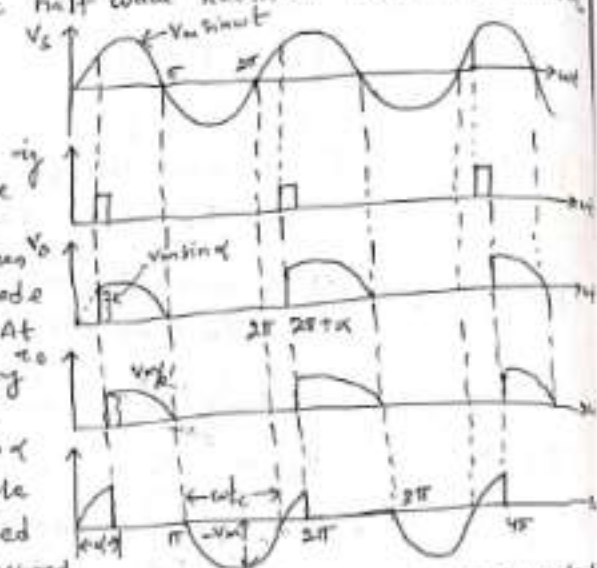
## **MODULE- III**

## Phase controlled Rectifier



At some delay angle  $\alpha$ , a positive gate signal applied between the gate and cathode turns on the SCR. At the instant of delay angle  $\alpha$ ,  $v_o$  rises from zero to  $v_m \sin \alpha$ .

A firing angle may thus be defined as the angle measured from the instant that gives the largest average output voltage to the instant it is triggered.



† Thyristor conducts from  $\omega t = \alpha$  to  $\pi$ ,  $2\pi + \alpha$  to  $3\pi$  and so on. Over the firing angle delay of  $\alpha$ , load voltage  $v_o = 0$  but during conduction angle  $(\pi - \alpha)$ ,  $v_o = v_s$ .

† As firing angle is increased from zero to  $\pi$ , the average load voltage decreases from the largest value to zero.

† As thyristor is reversed biased for  $\pi$  radians, the circuit turn-off time is given by  $t_c = \frac{\pi}{\omega}$  sec.

† The circuit turn-off time  $t_c$  must be greater than the SCR turn-off time  $t_{q}$ .

Average voltage  $V_o$  across load  $R$

$$V_o = \frac{1}{2\pi} \int_{\alpha}^{\pi} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{2\pi} (1 + \cos \alpha)$$

The maximum value of  $V_o$  occurs at  $\alpha = 0$

$$V_{max} = \frac{V_m}{2\pi} \cdot 2 = \frac{V_m}{\pi}$$

Average load current  $I_o = \frac{V_o}{R} = \frac{V_m}{2\pi R} (1 + \cos\alpha)$

R.m.s output voltage  $V_{rms} = \left[ \frac{1}{2\pi} \int_{\alpha}^{\pi} V_m^2 \sin^2 \omega t \cdot d(\omega t) \right]^{1/2}$

$$= \frac{V_m}{2\sqrt{\pi}} \left[ \pi - \alpha + \frac{1}{2} \sin 2\alpha \right]^{1/2}$$

Rms value current  $I_{rms} = \frac{V_{rms}}{R}$

Power delivered to load = (rms load voltage) (rms load current)

$$= V_{rms} I_{rms} = \frac{V_{rms}^2}{R} = I_{rms} R$$

input voltampere = (rms source voltage) (total rms line current)

$$= V_s I_{rms} = V_s \cdot \frac{V_{rms}}{R} = \frac{V_s}{R} \frac{V_m}{2\sqrt{\pi}} \left[ \pi - \alpha + \frac{1}{2} \sin 2\alpha \right]^{1/2}$$

$$= \frac{V_s \cdot \sqrt{2} V_s}{2\sqrt{\pi} R} \left[ \pi - \alpha + \frac{1}{2} \sin 2\alpha \right]^{1/2}$$

$$= \frac{\sqrt{2} V_s^2}{2R\sqrt{\pi}} \left[ \pi - \alpha + \frac{1}{2} \sin 2\alpha \right]^{1/2}$$

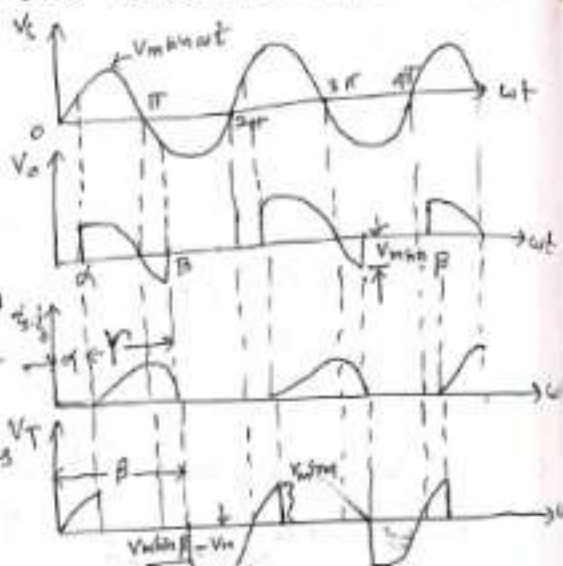
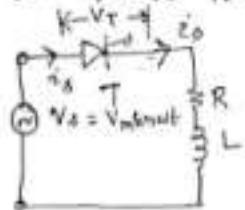
input power factor =  $\frac{\text{power delivered to load}}{\text{input VA}}$

$$= \frac{V_{rms} \cdot I_{rms}}{V_s \cdot I_{rms}} = \frac{V_{rms}}{V_s}$$

L  
Always  
for.

$$Pf = \frac{1}{\sqrt{2} \pi} \left[ \pi - \alpha + \frac{1}{2} \sin 2\alpha \right]^{1/2}$$

### Single phase half wave circuit with R-L load.



At  $\omega t = \alpha$  thyristor is turned on by getting signal. The load voltage  $v_o$  at once becomes equal to source voltage  $V_s$ . The

inductance  $L$  forces the load, or output current  $i_o$  to rise gradually.  $i_o$  rises to maximum value and then decrease. At  $\omega t = \pi$   $v_o$  is zero but  $i_o$  is not zero because due to load inductance. After  $\omega t = \pi$ , SCR subjected to reverse voltage but it will not turned off. It will turned off at  $\omega t = \beta$ . when  $\beta > \pi$   $i_o$  reduces to zero. SCR is turned off. At  $\omega t = \beta$   $V_o = 0$   $i_o = 0$ .

At  $\omega t = 2\pi + \alpha$ , SCR is triggered again.  $\beta$  is called extinction angle  $(\beta - \alpha) = \gamma$  is called conduction angle. At  $\omega t = \alpha$   $V_T = V_m \sin \alpha$ . The circuit turn off time  $t_c = \frac{2\pi - \beta}{\omega}$

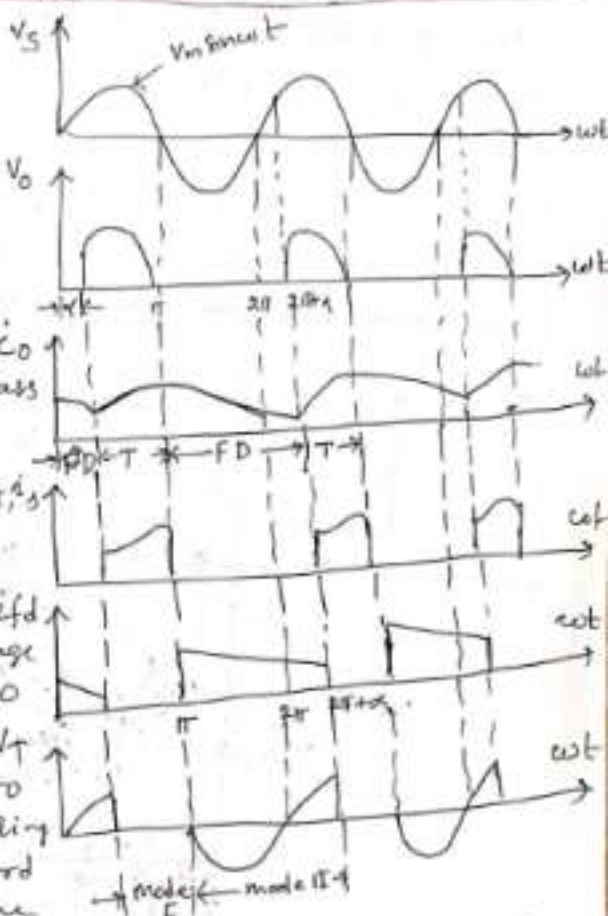
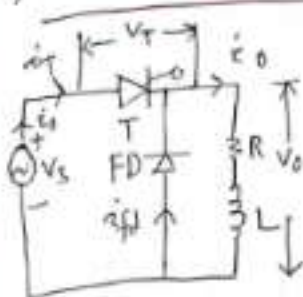
$$V_o = \frac{1}{2\pi} \int_{\alpha}^{\beta} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{2\pi} (\cos \alpha - \cos \beta)$$

$$I_o = \frac{V_m}{2\pi R} (\cos \alpha - \cos \beta)$$

$$\text{RMS load voltage} = \left[ \frac{1}{2\pi} \int_{\alpha}^{\beta} V_m^2 \sin^2 \omega t \, d(\omega t) \right]^{1/2}$$

$$\frac{V_m}{2\sqrt{\pi}} \left[ \beta - \alpha - \frac{1}{2} (\sin 2\beta - \sin 2\alpha) \right]^{1/2}$$

# Single phase half wave circuit with R-L load and Free-wheeling diode



A free-wheeling diode is also called by pass or commutating diode. At firing angle of  $\alpha$ , SCR is triggered, so source voltage appears across the load voltage  $V_o$ . At  $\omega t = \pi$ ,  $V_o = 0$  and just after  $V_s$  tends to reverse, free wheeling diode FD is forward biased through the conducting SCR. As a result, load current  $i_o$  is immediately transferred from SCR to FD, as  $V_s$  tends to reverse. During free wheeling period load current does not decay to zero until SCR is triggered again  $\pi + \alpha$ . Voltage drop across FD is almost zero. Load voltage is zero during free-wheeling period. Therefore circuit turn-off time  $t_c = \frac{\pi}{\omega}$  sec.

Therefore circuit turn-off time  $t_c = \frac{\pi}{\omega}$  sec.

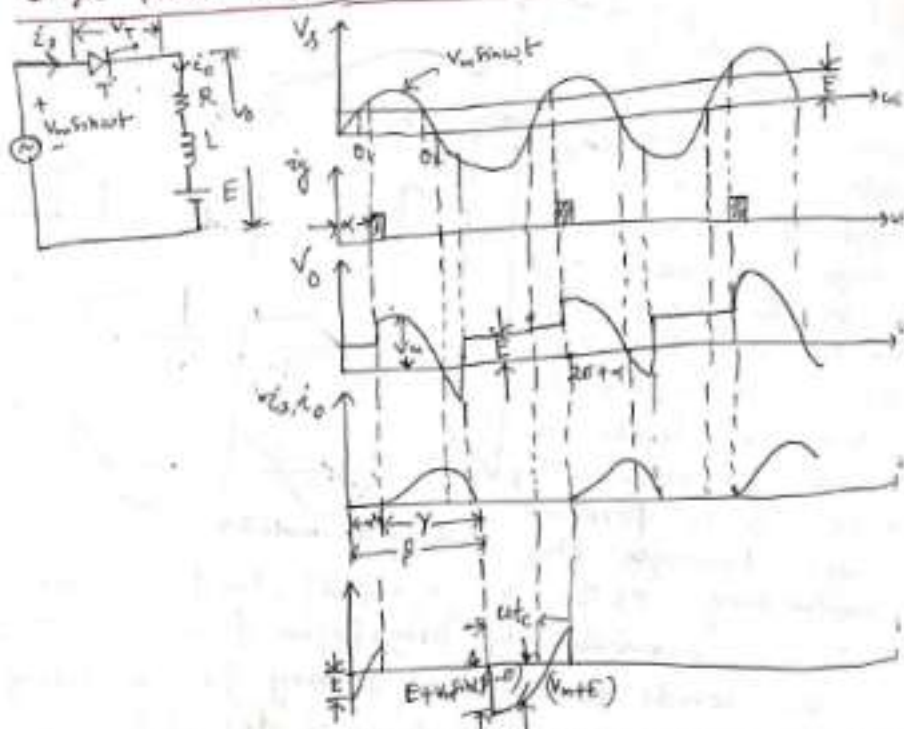
Average load voltage

$$V_o = \frac{1}{2\pi} \int_{\alpha}^{\pi} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{2\pi} (1 + \cos \alpha)$$

Average load current  $I_o = \frac{V_o}{R} = \frac{V_m}{2\pi R} (1 + \cos \alpha)$

Advantages of FD

- (i) input pf improved
  - (ii) load current waveform is improved.
  - (iii) load performance is better.
- Single phase half-wave circuit with R-L-E load



A single phase half-wave controlled converter with R-L-E load. The counter emf  $E$  in the load may be due to a battery or a dc motor. The minimum value of firing angle is obtained from the relation

$$V_m \sin \alpha = E \quad \alpha_1 = \sin^{-1}(E/V_m)$$

In case thyristor  $T$  is fired at an angle  $\alpha < \alpha_1$ , then  $E > V_s$ , SCR is reverse biased and there is

it will not turn on. Maximum value of firing angle is  $\theta_2 = \pi - \theta_1$

$$I_o = \frac{1}{2\pi R} \left[ \int_{\alpha}^{\beta} (V_m \sin \omega t - E) d(\omega t) \right]$$

$$= \frac{1}{2\pi R} \left[ V_m (\cos \alpha - \cos \beta) - E(\beta - \alpha) \right]$$

$$\gamma = \beta - \alpha \quad \beta = \gamma + \alpha$$

$$I_o = \frac{1}{2\pi R} \left[ V_m [\cos \alpha - \cos(\gamma + \alpha)] - E \cdot \gamma \right]$$

Power delivered to load =  $I_{rms}^2 R + I_o E$

$$\text{Supply power factor} = \frac{I_{rms}^2 R + I_o E}{V_s I_{rms}}$$

circuit turn-off time is  $\frac{2\pi - \beta}{\omega}$  sec.

Problem A dc battery is charged through a resistor  $R$ . Derive an expression for the average value of charging current in terms of  $V_m, E, R$  taken on the assumption that SCR is fired continuously.

(a) For an ac source voltage of 230V, 50 Hz, find the value of average charging current for  $R = 8 \Omega$  and  $E = 150V$ .

(b) Find the power supplied to battery and that dissipated in the resistor.

(c) Calculate supply PF.

$$I_o = \frac{1}{2\pi R} \left[ \int_{\theta_1}^{\pi - \theta_1} (V_m \sin \omega t - E) d(\omega t) \right]$$

$$= \frac{1}{2\pi R} \left[ 2V_m \cos \theta_1 - E(\pi - 2\theta_1) \right]$$

$$\theta_1 = \sin^{-1} \frac{E}{V_m} = \sin^{-1} \frac{150}{\sqrt{2} \times 230} = 27.46^\circ$$

$$I_o = \frac{1}{2\pi \cdot 8} \left[ 2 \times \sqrt{2} \times 230 \times \cos 27.46^\circ - 150 \left( \pi - \frac{2 \times 27.46^\circ}{180} \times \pi \right) \right]$$

$$= 4.9676 \text{ A}$$

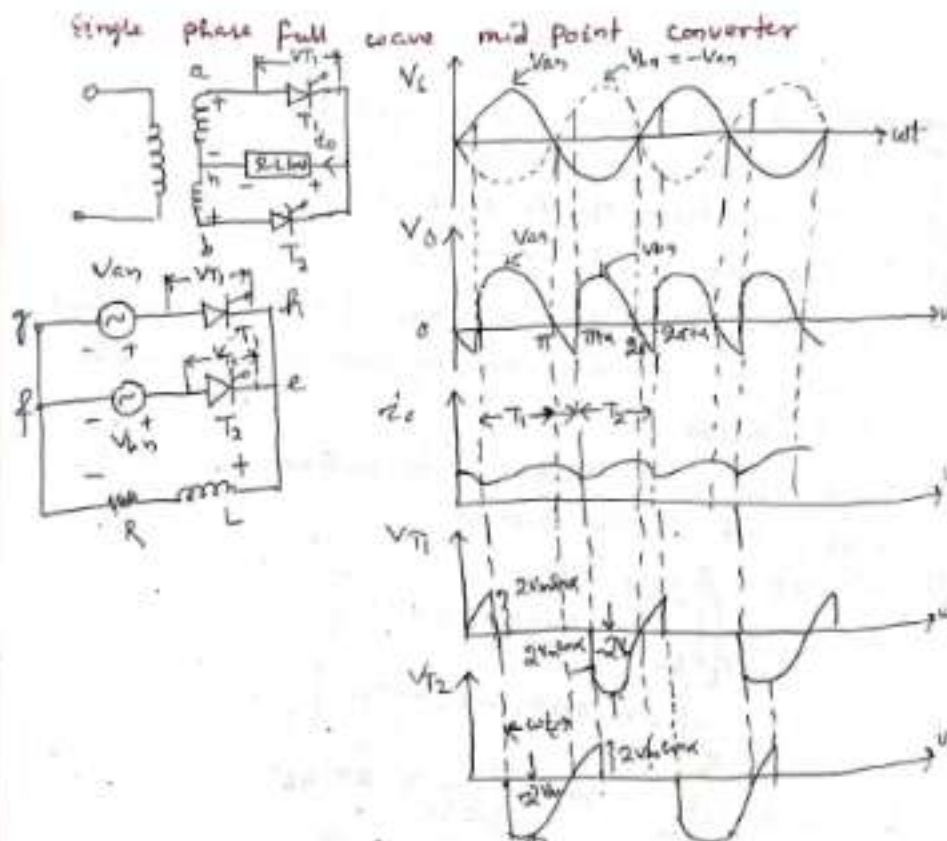
(b) Power supplied to battery =  $E I_0 = 150 \times 4.96 = 744.6$   
 For finding the power dissipated in  $R$ , rms value of charging current must be obtained

$$I_{rms} = \left[ \frac{1}{2\pi \cdot 64} \left\{ (160^2 + 230^2) \left( \pi - 2 \times 27.466 \times \frac{\pi}{180} \right) + 230^2 \cos 27.466^\circ \right\} \right]^{1/2}$$

$$= 9.2955 \text{ A}$$

$\therefore$  power dissipated in resistor =  $(9.2955)^2 \times 2 = 691.25$

(c) Supply pf =  $\frac{691.25 + 745.14}{230 \times 9.2955} = 0.672$  lagging



When terminal a is positive with respect to n, terminal n is positive with respect to b. Therefore  $V_{cn} = V_{bn}$   
 $V_{an} = -V_{bn}$ , Thyristor  $T_1$  and  $T_2$  are forward biased during positive and negative half cycle.

At delay angle  $\alpha$ ,  $T_1$  gets turned on. At firing angle  $\alpha$ , supply voltage  $2V_m \sin \alpha$  reverse biases  $T_2$ , this SCR is therefore turned off. Here  $T_1$  is called the incoming thyristor and  $T_2$  the outgoing thyristor. As incoming SCR is triggered, ac supply voltage applies reverse bias across the outgoing thyristor and turn it off. Load current is also transferred from outgoing SCR to incoming SCR. This process of SCR turn-off by natural reversal of ac supply voltage is called natural or line commutation.

$$V_{an} = V_m \sin \omega t \quad V_{bn} = -v_{bn} = -V_m \sin \omega t$$

$$V_{ab} = V_{an} + V_{bn} = 2V_m \sin \omega t$$

By applying KVL to the loop efghe of the equivalent circuit at the instant  $T_1$  is triggered.

$$V_{T_2} - V_{bn} + V_{T_1} = 0$$

$$V_{T_2} = V_{bn} - V_{an} + V_{T_1}$$

with  $T_1$  conducting  $V_{T_1} = 0$

$$V_{T_2} = -V_m \sin \omega t - V_m \sin \alpha = -2V_m \sin \alpha$$

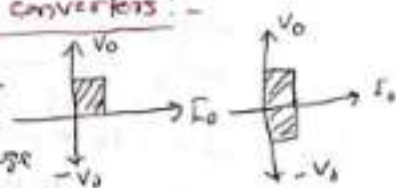
Therefore, SCR turn off time as  $t_c = \frac{2(\pi - (\pi + \alpha))}{\omega} = \frac{\pi - \alpha}{\omega}$

The circuit turn-off time must be greater than SCR turn-off time.

$$V_0 = \frac{1}{\pi} \int_{\alpha}^{\pi + \alpha} V_m \sin \omega t \, d(\omega t) = \frac{2V_m \cos \alpha}{\pi}$$

### single phase full wave Bridge converters:-

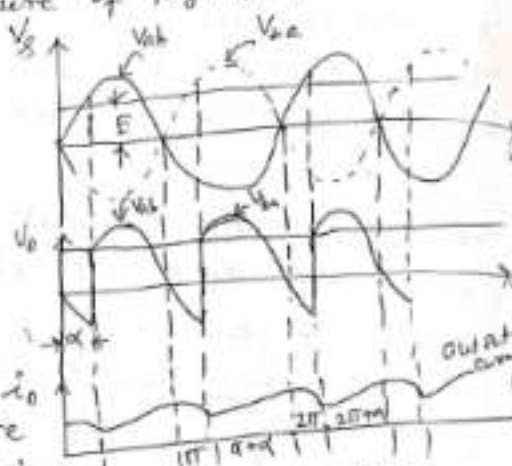
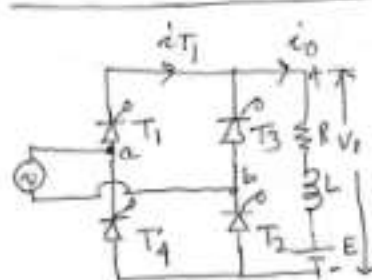
1. An uncontrolled converter or rectifier uses only diodes and the level of dc output voltage can not be controlled.



2. A half-controlled converter or semiconverter uses a mixture of diodes and thyristors and there is a limited control over the level of dc output

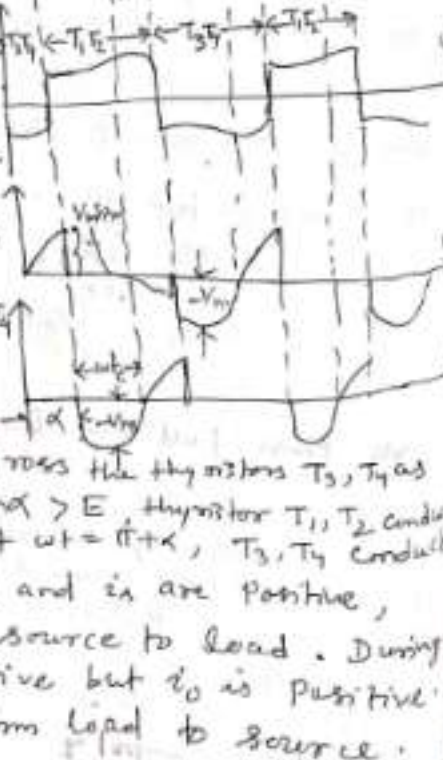
voltage. A fully-controlled converter or full converter uses thyristors only and there is wider control over level of dc output voltage. A semiconverter is one-quadrant converter. A one-quadrant converter has one polarity of dc output voltage and current at its out terminals. A two quadrant converter is one in which voltage polarity can reverse because of the unidirectional nature of thyristors.

1 $\phi$  full wave converter



The load is assumed to be of RLE type, where E is the load circuit emf. Voltage E may be due to a battery in the load circuit or may be generated emf of dc motor. Load current  $i_o$  is assumed continuous over the working voltage.

At  $\omega t = \alpha$ ,  $V_{ab}$  is positive thyristor  $T_1, T_2$  conducts. Supply voltage  $v_m \sin \omega t$  immediately appears across the thyristors  $T_3, T_4$  as reverse bias. If  $v_m \sin \omega t > E$ , thyristor  $T_1, T_2$  conduct from  $\omega t = \alpha$  to  $\pi + \alpha$ , At  $\omega t = \pi + \alpha$ ,  $T_3, T_4$  conduct. During  $\alpha$  to  $\pi$ , both  $V_o$  and  $i_o$  are positive, power will flow from source to load. During  $\pi$  to  $\pi + \alpha$   $V_o$  is negative but  $i_o$  is positive. Load current flows from load to source.



but net power flow is from ac source to dc load because  $(\pi - \alpha) > \alpha$ . The average output voltage of full converter.

$$V_o = \frac{1}{\pi} \int_{\alpha}^{\pi + \alpha} V_m \sin \omega t d(\omega t) = \frac{2V_m}{\pi} \cos \alpha$$

(ii) If  $\alpha > 90^\circ$   $V_o$  is negative.  $V_o$  is negative. If the load circuit emf  $E$  is reversed this source  $E$  will feed power back to ac supply. This operation of full converter is known as inverter operation. The full converter with firing angle delay greater than  $90^\circ$  is called line commutated inverter. Such an operation is used in the regenerative braking mode of dc motor. But net power flow is from dc source to ac source, because  $(\pi - \alpha) < \alpha$ .

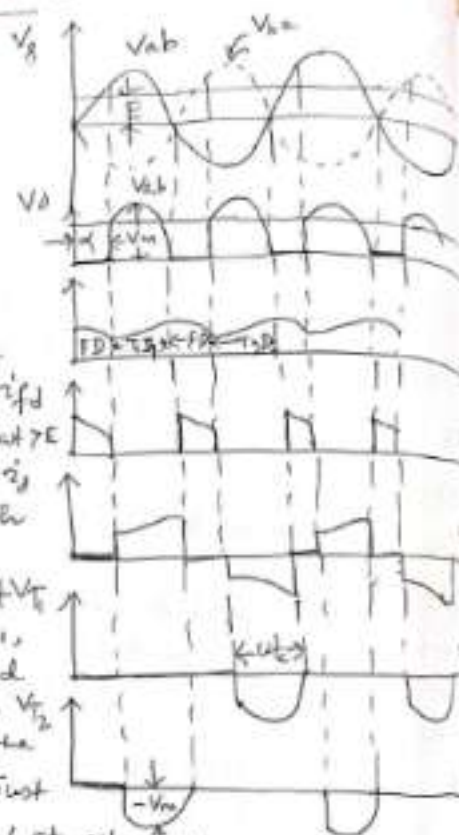
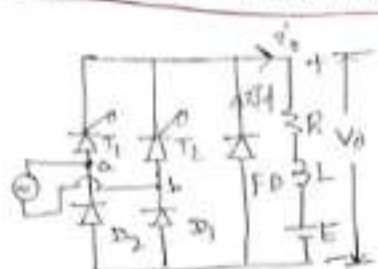
\* For converter operation  $V_o > E$  and for inverter operation  $E > V_o$ .

\* Circuit turn-off time  $t_c = \frac{\pi - \alpha}{\omega}$ .

\* Piv rating is  $2V_m$  for mid point converter and  $V_m$  for full converter.

\* Power handled by mid-point configuration is about half of that handled by bridge configuration.

# Single phase semiconverter :-



A single phase semiconverter with two thyristors and three diodes. At  $\omega t = \alpha$ ,  $T_1$  is forward biased when  $V_m \sin \omega t > E$ . With  $T_1$  on, load gets  $i_o$  connected to source through  $T_1$  and  $D_1$ . For the period  $\omega t = \alpha$  to  $\pi$ , load current  $i_o$  flows through  $RLE, D_1$ , source and  $T_1$ , and load terminal voltage  $V_o$  is of  $V_m/2$  the same waveform as the ac source voltage  $V_s$ . Just as  $V_o$  tends to reverse (at  $\omega t = \pi$ ),

$FD$  is forward biased and starts conducting. The load current  $i_o$  is transferred from  $T_1, D_1$  to  $FD$ .  $T_1$  is turned off at  $\omega t = \pi$ . The load terminal are short circuited through  $FD$ , therefore load or output voltage  $V_o$  is zero during  $\pi < \omega t < \pi + \alpha$ .

For semiconductors, the average output voltage

$$V_o = \frac{1}{\pi} \int_{\alpha}^{\pi} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{\pi} (1 + \cos \alpha)$$

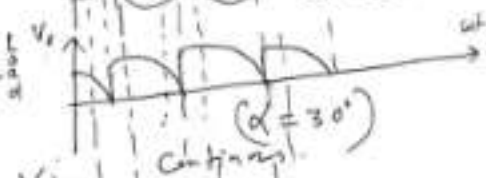
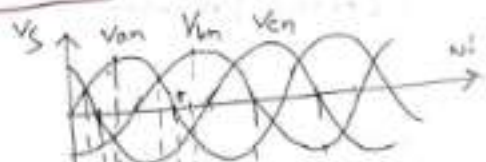
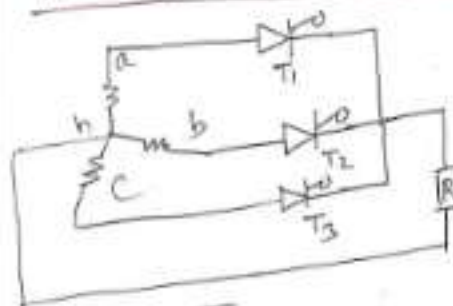
The circuit turn off time for the semiconverter

$$t_c = \frac{\pi - \alpha}{\omega} \text{ sec.}$$

### 3 phase converters

1. In 3-phase converters, the ripple frequency of the converter output voltage is higher than in single phase converter. Consequently, the filtering requirement for smoothing out the load current are less.
2. The load current is mostly continuous in 3 phase converters. The load performance, when 3-phase converters are used, is therefore superior as compared to when single phase converters are used.

### Three phase halfwave converters with R load



$$V_o = \frac{3}{2\pi} \int_{\pi/6 + \alpha}^{\pi} \sqrt{3} V_m \sin \omega t \, d(\omega t)$$

$$= \frac{3\sqrt{3}V_m}{2\pi} \left[ 1 + \cos\left(\alpha + \frac{\pi}{6}\right) \right]$$

For R-L load

$$V_o = \frac{3}{2\pi} \int_{\pi/6 + \alpha}^{\frac{5\pi}{6} + \alpha} \sqrt{3} V_m \sin \omega t \, d(\omega t)$$

$$= \frac{3\sqrt{3}V_m}{2\pi} \cos \alpha$$

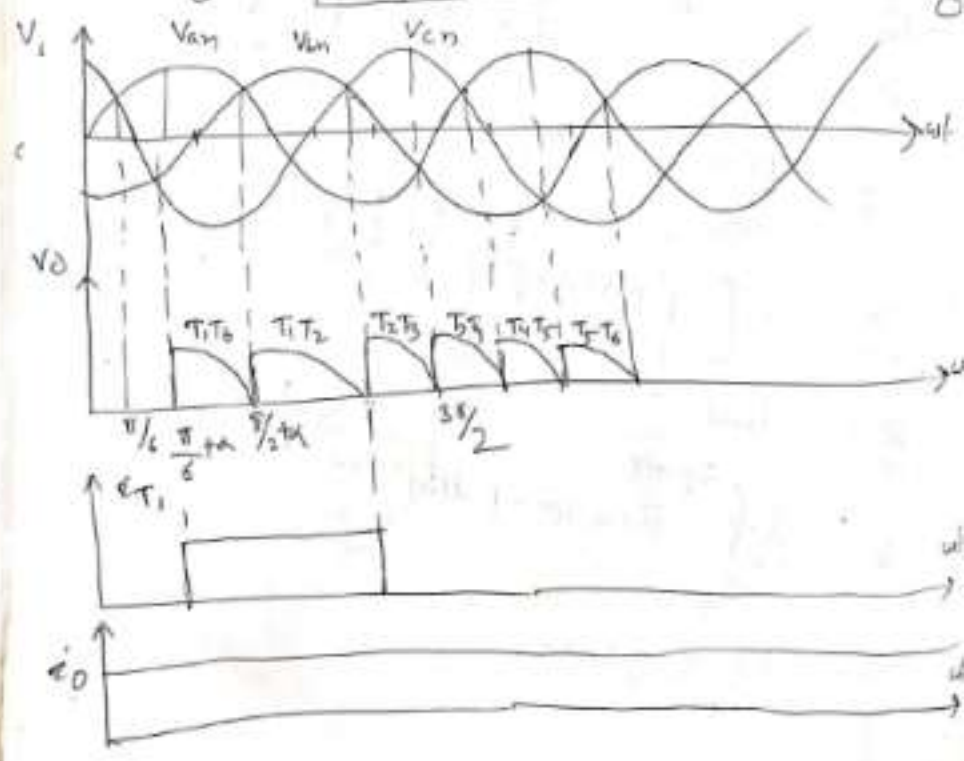
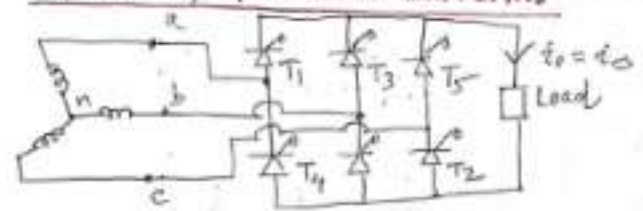
Rms output voltage is found from

$$V_{\text{rms}} = \left[ \frac{3}{2\pi} \int_{\frac{\pi}{6} + \alpha}^{\frac{5\pi}{6} + \alpha} V_m^2 \sin^2 \omega t \, d(\omega t) \right]$$

$$= \sqrt{3} V_m \left( \frac{1}{6} + \frac{\sqrt{3}}{8\pi} \cos 2\alpha \right)$$

for when thyristor  $T_1$  is fired at  $\omega t = \frac{\pi}{6} + \alpha$ , the phase voltage  $V_{an}$  appears across the load until  $T_1$  is fired at  $\omega t = \frac{5\pi}{6} + \alpha$ , when  $T_2$  is fired thyristor  $T_1$  is reversed biased, because the line to line voltage  $V_{ab} (= V_{an} - V_{bn})$

3 $\phi$  (Phase) Full-wave converters



Three-phase converters are extensively used in industrial applications up to the 120-kw level, where two quadrant operation is required. This circuit is known as three phase bridge. The thyristors are fired at an interval of  $\pi/3$ . The frequency of ripple voltage is  $6f_s$  and the filtering requirement is less than that of three-phase semi and half-wave converters.

At  $\omega t = \pi/6 + \alpha$ , Thyristor  $T_6$  is already conducting and thyristor  $T_1$  is turned on. During interval  $\pi/6 + \alpha$  to  $\pi/2 + \alpha$ , thyristor  $T_1, T_6$  conduct and line to line voltage  $V_{ab} (= V_{an} - V_{bn})$  appears across the load. At  $\omega t = \pi/2 + \alpha$ , thyristor  $T_2$  is fired and  $T_6$  is reversed biased immediately.  $T_6$  turns off due to natural commutation. During  $\pi/2 + \alpha$  to  $5\pi/6 + \alpha$ , Thyristor  $T_1$  and  $T_2$  conduct and line to line voltage appears across the load. If the thyristors are numbered 1, 2, 3, 4, 5, 6 and 6

$$V_{an} = V_m \sin \omega t$$

$$V_{bn} = V_m \sin (\omega t - 2\pi/3)$$

$$V_{cn} = V_m \sin (\omega t + 2\pi/3)$$

$$V_{ab} = V_{an} - V_{bn} = \sqrt{3} V_m \sin (\omega t + \pi/6)$$

The average output voltage is found from

$$V_{dc} = \frac{3}{\pi} \int_{\pi/6 + \alpha}^{\pi/2 + \alpha} \sqrt{3} V_m \sin (\omega t + \pi/6) dt$$

$$V_{dc} = \frac{3\sqrt{3} V_m}{\pi} \cos \alpha$$

$$V_{rms} = \left[ \frac{3}{\pi} \int_{\pi/6 + \alpha}^{\pi/2 + \alpha} 3 V_m^2 \sin^2 (\omega t + \pi/6) d(\omega t) \right]^{1/2}$$

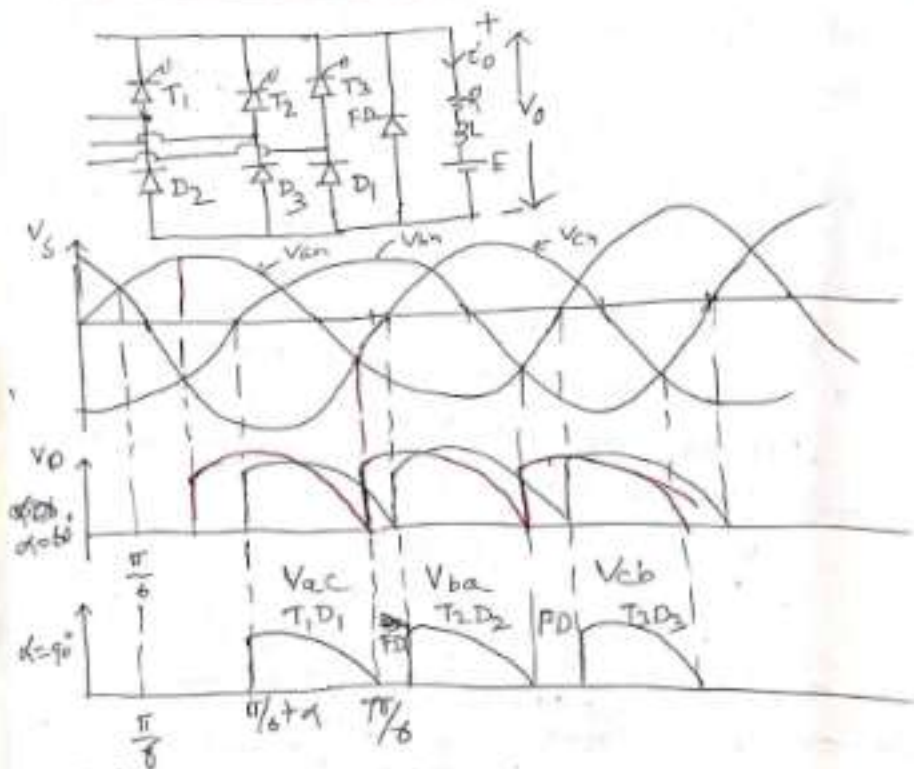
$$= \sqrt{3} V_m \left( \frac{1}{2} + \frac{3\sqrt{3}}{4\pi} \cos 2\alpha \right)^{1/2}$$

In case output current is assumed constant at  $I_0$ , the rms value of source current is

$$I_s = \sqrt{I_0^2 \frac{2\pi}{3} \times \frac{1}{\pi}} = I_0 \sqrt{\frac{2}{3}}$$

rms value of thyristor current =  $\sqrt{I_0^2 \frac{2\pi}{3} \times \frac{1}{2\pi}} = I_0 \sqrt{\frac{1}{3}}$

### Three phase semiconverters :-



It is a one quadrant operation. The power factor of the converter decreases as the delay angle increases. Three phase semiconverter with a highly inductive load and load current has negligible ripple current. The frequency of output voltage is  $3f_s$ . During the period  $\pi/6$  to  $7\pi/6$  thyristor  $T_1$  forward bias. If  $T_1$  is fired at  $\omega t = \pi/6 + \alpha$ ,  $T_1$  and  $D_1$  conduct and line to o.c.

$V_{c1}$  stress negative and free wheeling diode  $D_{m1}$  conducts. The load current continues to flow through  $D_{m1}$  and  $T_1$  and  $D_1$  are turned off. If  $\alpha < \pi/3$  each thyristor conducts for  $2\pi/3$  and free wheeling diode  $D_{m1}$  does not conduct.

$$V_{a1} = V_m \sin \omega t$$

$$V_{b1} = V_m \sin(\omega t - 2\pi/3)$$

$$V_{c1} = V_m \sin(\omega t + 2\pi/3)$$

$$V_{ac} = V_{a1} - V_{c1} = \sqrt{3} V_m \sin(\omega t - \pi/6)$$

$$V_{dc} = \frac{3}{2\pi} \int_{\pi/6 + \alpha}^{7\pi/6} V_{ac} d(\omega t) = \frac{3}{2\pi} \int_{\pi/6 + \alpha}^{7\pi/6} \sqrt{3} V_m \sin(\omega t - \pi/6) d(\omega t)$$

$$= \frac{3\sqrt{3} V_m}{2\pi} (1 + \cos \alpha)$$

$$V_{rms} = \left[ \frac{3}{2\pi} \int_{\pi/6 + \alpha}^{7\pi/6} 3 V_m^2 \sin^2(\omega t - \pi/6) d(\omega t) \right]^{1/2}$$

$$= \sqrt{3} V_m \left[ \frac{3}{4\pi} (\pi - \alpha + \frac{1}{2} \sin 2\alpha) \right]^{1/2}$$

for  $\alpha < \pi/3$  and continuous output voltage.

$$V_{dc} = \frac{3}{2\pi} \int_{\pi/6 + \alpha}^{\pi/2} V_{ab} d(\omega t) + \int_{\pi/2}^{5\pi/6 + \alpha} V_{ac} d(\omega t)$$

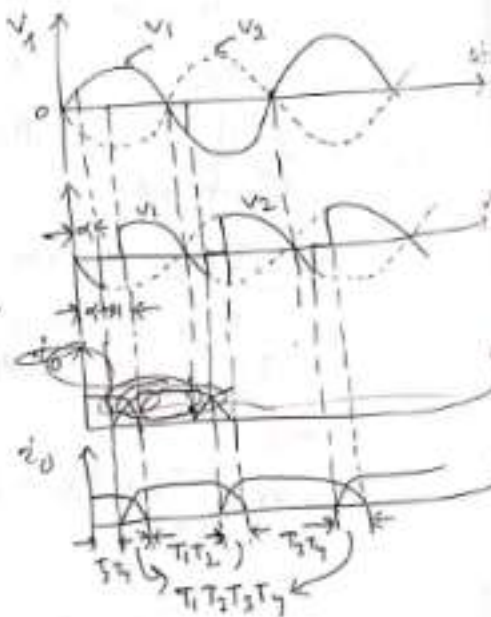
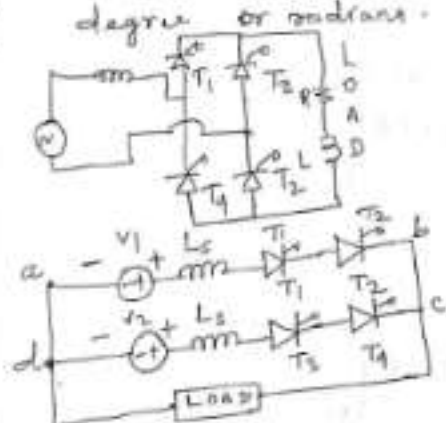
$$= \frac{3\sqrt{3} V_m}{2\pi} (1 + \cos \alpha)$$

$$V_{rms} = \left[ \frac{3}{2\pi} \int_{\pi/6 + \alpha}^{\pi/2} V_{ab}^2 d(\omega t) + \int_{\pi/2}^{5\pi/6 + \alpha} V_{ac}^2 d(\omega t) \right]^{1/2}$$

$$= \sqrt{3} V_m \left[ \frac{3}{4\pi} \left( \frac{2\pi}{3} + \sqrt{3} \cos^2 \alpha \right) \right]^{1/2}$$

## Effect of source impedance on the performance of converter

1. If the source impedance is resistive, then there will be a voltage drop across the resistance and the average voltage of a converter gets reduced by an amount equal to  $E_{0s}$  for single phase converter and  $2E_{0s}$  for 3 phase converter. It is the constant dc load current and  $r_s$  is the source resistance per phase.
2. The source inductance causes the outgoing and incoming SCR to conduct together. During the commutation period, the output voltage is equal to the average value of the conducting-phase voltage. For a single phase converter, the load voltage is equal to the average value of the conducting phase voltage. For a 3-phase converter, the load voltage will be zero and for a 3-phase converter, the load voltage is  $(v_2 + v_3)/2$ . The commutation period in seconds, when outgoing and incoming SCR are conducting, is known as overlap period. The angular period during which both the incoming and outgoing SCR are conducting is known as commutation angle or overlap angle  $\mu$  in degree or radians.



$$L_s \frac{di_1}{dt} - L_s \frac{di_2}{dt} - v_2 - v_1 = 0$$

$$L_s \frac{di_1}{dt} - L_s \frac{di_2}{dt} = v_1 - v_2$$

$$L_s \frac{di_1}{dt} - L_s \frac{di_2}{dt} = v_m \sin \omega t + v_m \sin \omega t$$

$$L_s \left( \frac{di_1}{dt} - \frac{di_2}{dt} \right) = 2v_m \sin \omega t$$

$$\frac{di_1}{dt} - \frac{di_2}{dt} = \frac{2v_m}{L_s} \sin \omega t$$

$$i_1 + i_2 = I_0$$

$$\frac{di_1}{dt} + \frac{di_2}{dt} = 0 \quad \therefore \frac{di_1}{dt} = -\frac{di_2}{dt}$$

$$\frac{di_1}{dt} + \frac{di_1}{dt} = \frac{2v_m}{L_s} \sin \omega t$$

$$2 \frac{di_1}{dt} = \frac{2v_m}{L_s} \sin \omega t$$

$$\frac{di_1}{dt} = \frac{v_m}{L_s} \sin \omega t$$

$$i_1 = \frac{v_m}{L_s} \int \sin \omega t \, dt$$

$$I_0 = \frac{v_m}{\omega L_s} \left[ \cos \omega t \right]_{\alpha/\omega}^{(\alpha+\pi)/\omega} = \frac{v_m}{\omega L_s} \left[ \cos \omega \frac{\alpha+\pi}{\omega} + \cos \omega \frac{\alpha}{\omega} \right]$$

$$= \frac{v_m}{\omega L_s} \left[ -\cos(\alpha+\pi) + \cos \alpha \right]$$

$$= \frac{v_m}{\omega L_s} \left[ \cos \alpha - \cos(\alpha+\pi) \right]$$

$$V_0 = \frac{v_m}{2\pi} \int_{\alpha+\pi}^{\alpha} \sin \omega t \cdot d(\omega t) = \frac{v_m}{\pi} \left[ \cos(\alpha+\pi) - \cos \alpha \right]$$

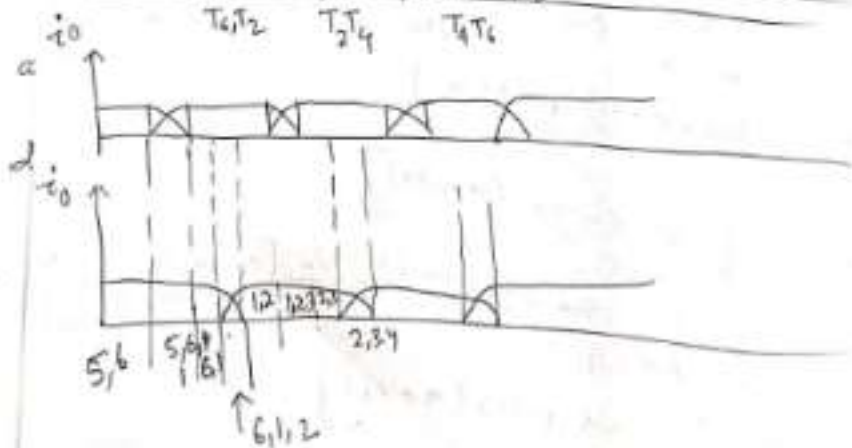
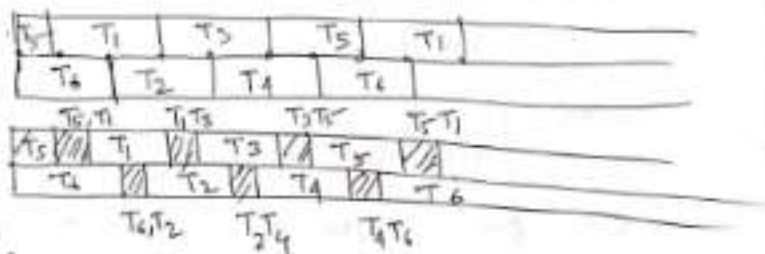
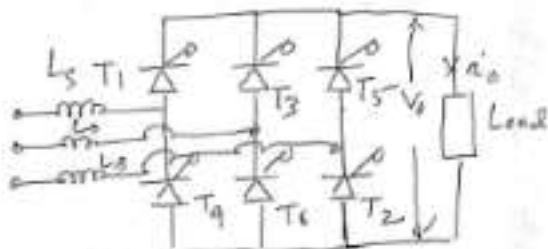
$$= \frac{v_m}{\pi} \left[ \cos \alpha + \cos(\alpha+\pi) \right]$$

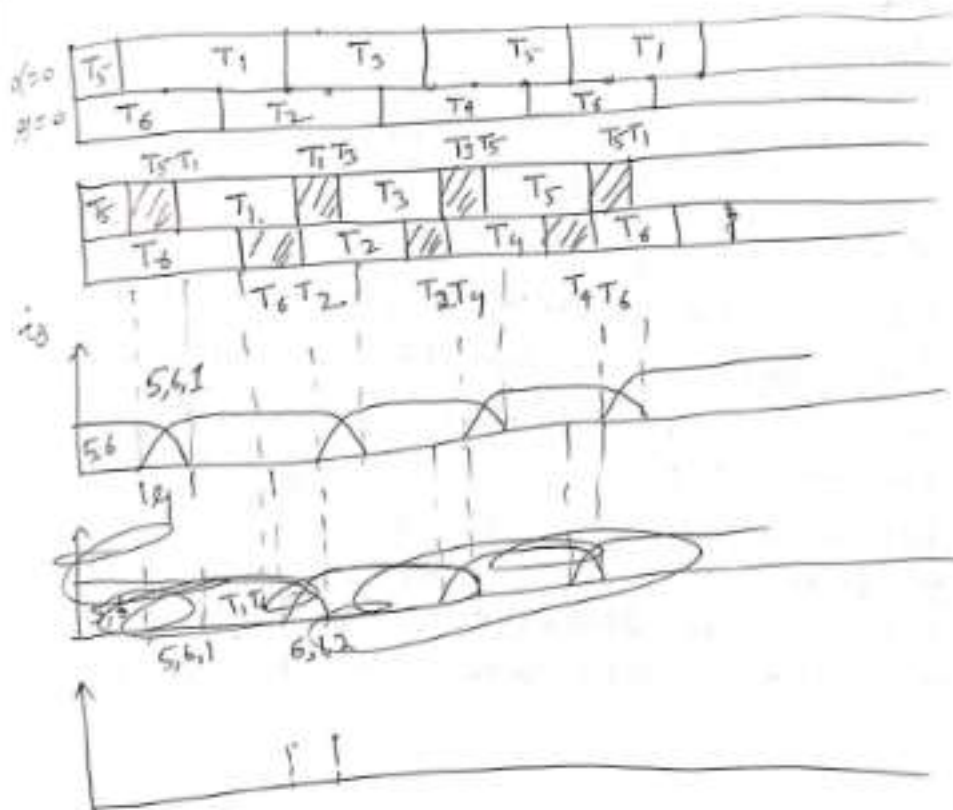
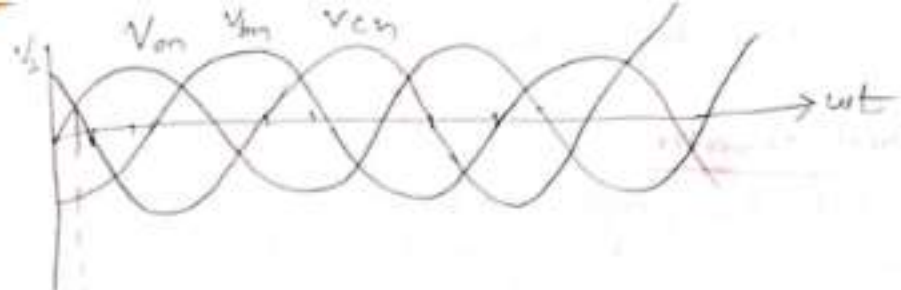
$$\cos(\alpha + \beta) = \cos \alpha - \frac{\omega L_s E_o}{V_m}$$

$$\begin{aligned} \therefore V_o &= \frac{V_m}{\pi} \left[ \cos \alpha + \cos(\alpha + \beta) \right] \\ &= \frac{V_m}{\pi} \left[ \cos \alpha + \cos \alpha - \frac{\omega L_s E_o}{V_m} \right] \\ &= \frac{2 V_m}{\pi} \cos \alpha - \frac{V_m \omega L_s E_o}{\pi V_m} \end{aligned}$$

$$V_o = \frac{2 V_m}{\pi} \cos \alpha - \frac{\omega L_s E_o}{\pi}$$

Three phase full converter Bridge.





The average value of output voltage due to overlap

$$\begin{aligned}
 &= \frac{3}{\pi} \int_0^{\pi} v_L d(\omega t) = \frac{3}{\pi} \int_0^{\pi} L_s \frac{di}{dt} d(\omega t) \\
 &= \frac{3L_s}{\pi} \int_0^{\pi/\omega} \omega \frac{di}{dt} dt = \frac{3\omega L_s}{\pi} \int_0^{I_0} di \\
 &= \frac{3\omega L_s I_0}{\pi}
 \end{aligned}$$

output voltage with overlap =  $\frac{3\sqrt{3}V_m}{\pi} \cos\alpha - \frac{3\omega L I_d}{\pi}$

### Dual converter

With the firing angles controlled in a manner that  $\alpha_1 + \alpha_2 = 180^\circ$  and with both the converter operation, their average output voltage are equal and have the same polarity. One converter will be operating as rectifier with firing angle  $\alpha_1$  and the other as an inverter with firing angle  $(180^\circ - \alpha_1)$ . Though their average output voltage are equal, yet their instantaneous voltage  $V_{o1}$  and  $V_{o2}$  are out of phase in practical dual converter. This result in a voltage difference when the two converters are interconnected and as a consequence a large circulating current flows between the two converters but not through the load. In practical dual converters, this circulating current is limited to a tolerable value by inserting reactor between the two converters.

## **MODULE- IV**

## Inverters

→ A circuit that converts dc power into ac power at desired output voltage and frequency is called inverter.

Application:- adjustable-speed ac drives, induction heating, stand by air-craft power supplies, UPS (uninterruptible power supplies) for computers, hvdc transmission lines.

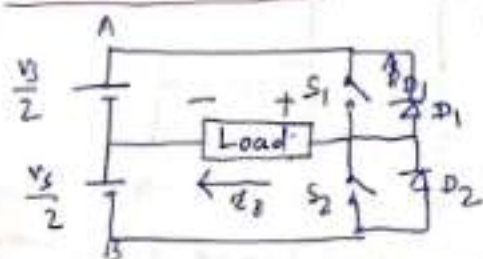
Configurations using ac to dc converters and dc to ac inverters are called dc-link inverters

Inverters can be broadly classified into two-types:-  
voltage source inverters and current source inverters.

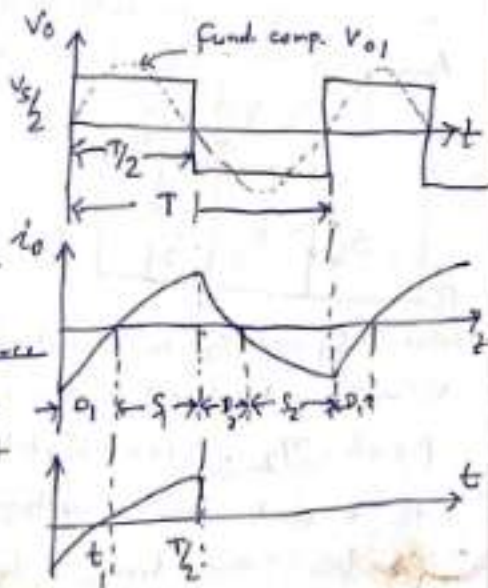
VSI:- voltage source inverter (VSI), is one in which the dc source has small or negligible internal impedance. It has stiff dc voltage source at its input terminals.

CSI A current source inverter (CSI) is fed with adjustable current from a dc source of high internal impedance. In CSI, fed with stiff current source, output current waves are not affected by the load.

### Half bridge VSI



When switch  $S_1$  is closed, source the current flows through the load  $V_s/2 - S_1 - \text{Load}$ . At time  $T/2$  the o/p voltage is  $V_s/2$ . When switch  $S_1$  is turned off  $S_2$  is turned on



The current flows  $V_s/2$  - Load -  $S_2$ . So the current flows through the load is anticlockwise direction. The o/p voltage is a square wave of amplitude is  $V_s/2$ .

R-Load: If the load is R, then waveform of load current  $i_o$  is also a square wave.

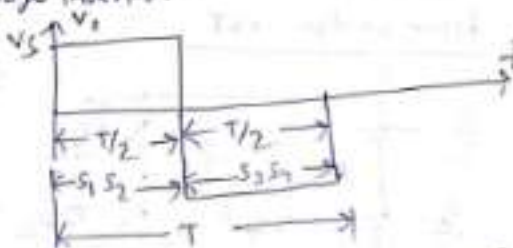
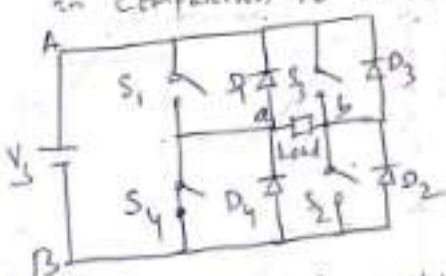
R-L load: - For R-L load, the load current cannot be in phase with load voltage. During the interval 0 to  $T/2$ , the o/p voltage  $V_o$  is positive. For time  $t$  to  $t_1$ , the o/p current  $i_o$  is negative.

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^{T/2} (V_s/2)^2 dt}$$

$$= \sqrt{\frac{1}{T} \times \frac{V_s^2}{4} \times T/2}$$

$$= \sqrt{\frac{V_s^2}{4}} = \frac{V_s}{2}$$

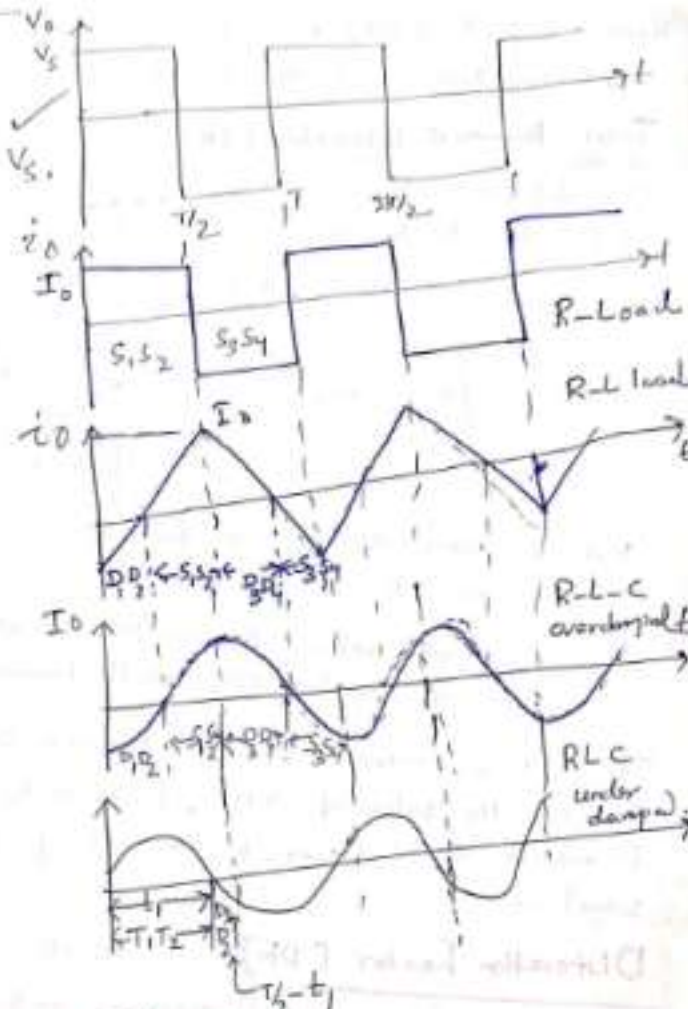
Full bridge inverter: - In this inverter the amplitude of output voltage is doubled whereas output power is four times in comparison to half-bridge inverter.



When  $S_1$  and  $S_2$  is switched on load current flows through  $V_s - S_1 - \text{load} - S_2 - V_s$ . Therefore, Load voltage  $V_o = V_s$  for period  $T/2$ . when switch  $S_3, S_4$  are on, A is connected to b and source voltage terminal B to load terminal a. Therefore, new load voltage  $V_o = -V_s$  from  $T/2$  to  $T$ .

$$V_{\text{rms}} = \sqrt{\frac{1}{T/2} \int_0^{T/2} v_s^2 dt}$$

$$\frac{2}{T} \times v_s^2 \times \frac{T}{2} = v_s$$



Performance parameters of inverters:-

Harmonic factor (HF<sub>n</sub>) :- It is defined as the ratio of rms value of n<sup>th</sup> harmonic voltage to the rms value of the fundamental voltage component.

$$HF_n = \left| \frac{V_{0n}}{V_{01}} \right|$$

V<sub>0n</sub> = rms value of n<sup>th</sup> harmonic component of output voltage.

V<sub>01</sub> = rms value of fundamental component of output voltage.

Harmonic factor (HF) is a measure of the contribution of any individual harmonic to the inverter output voltage.

### Total Harmonic Distortion (THD)

It is defined as the ratio of rms value of all the harmonic components, to the rms value of fundamental component.

$$THD = \frac{V_{oh}}{V_{o1}} = \frac{\sqrt{V_{os}^2 - V_{o1}^2}}{V_{o1}}$$

$$V_{oh} = \sqrt{V_{os}^2 - V_{o1}^2} = \left[ \left( \frac{V_{os}}{V_{o1}} \right)^2 - 1 \right]^{1/2}$$

$V_{oh}$  = rms value of all harmonic component present in the inverter output voltage.

$V_{os}$  = rms value of inverter output voltage including fundamental plus all the harmonics.

THD is a measure of total harmonic content in the waveform. Lower the value of THD, lower is the total harmonic content present and lower is amount of distortion in the waveform.

Distortion Factor (DF): - Distortion factor indicates the amount of harmonic that remains in the output voltage, after the harmonics in the output voltage have been subject to second order attenuation. It is defined as

$$DF = \frac{1}{V_{o1}} \left[ \sum_{n=3,5,7}^{\infty} \left( \frac{V_{on}}{n^2} \right)^2 \right]^{1/2}$$

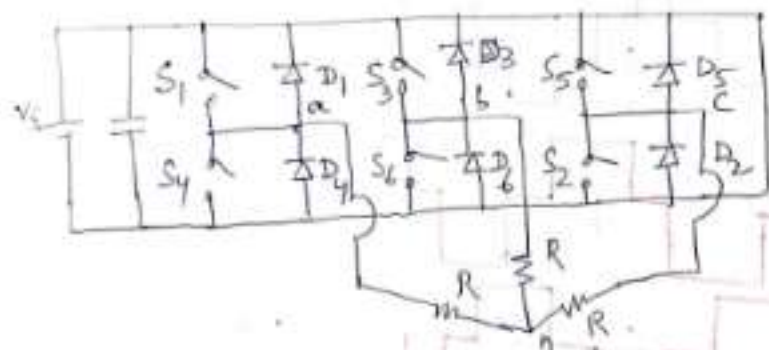
$$DF_n = \frac{V_{on}}{n^2 V_{o1}} \quad \checkmark$$

Lowest order harmonic (LOH): - The lowest frequency harmonic, whose output voltage magnitude is greater than or equal to 3% of fundamental component of

output voltage is called lowest order harmonics.

### Three phase inverters

- For providing adjustable-frequency power to industrial application three phase inverters are more common than single-phase inverters. A three phase inverter is a six-step bridge inverter. It uses a minimum six switches. In inverter terminology, a step is defined as a change in the firing from one switch to the next switch in proper sequence. For one cycle of  $360^\circ$ , each step would be of  $60^\circ$  interval for six-step inverter.



Three phase inverter consists of three half-bridge inverters arranged side by side. The gating signals of three half-bridge inverters should be displaced from each other by  $120^\circ$  so as to obtain 3-phase balanced voltage at the o/p terminals. A large capacitor connected at the input terminals tends to make the input dc voltage constant. The capacitor also suppresses the harmonics fed back to the dc source.

### Three Phase $180^\circ$ mode VSI

mode I (5, 6, 1) Thyristor conducts

$$R_{eq} = \frac{R^2}{2R} + R = \frac{3R}{2}$$

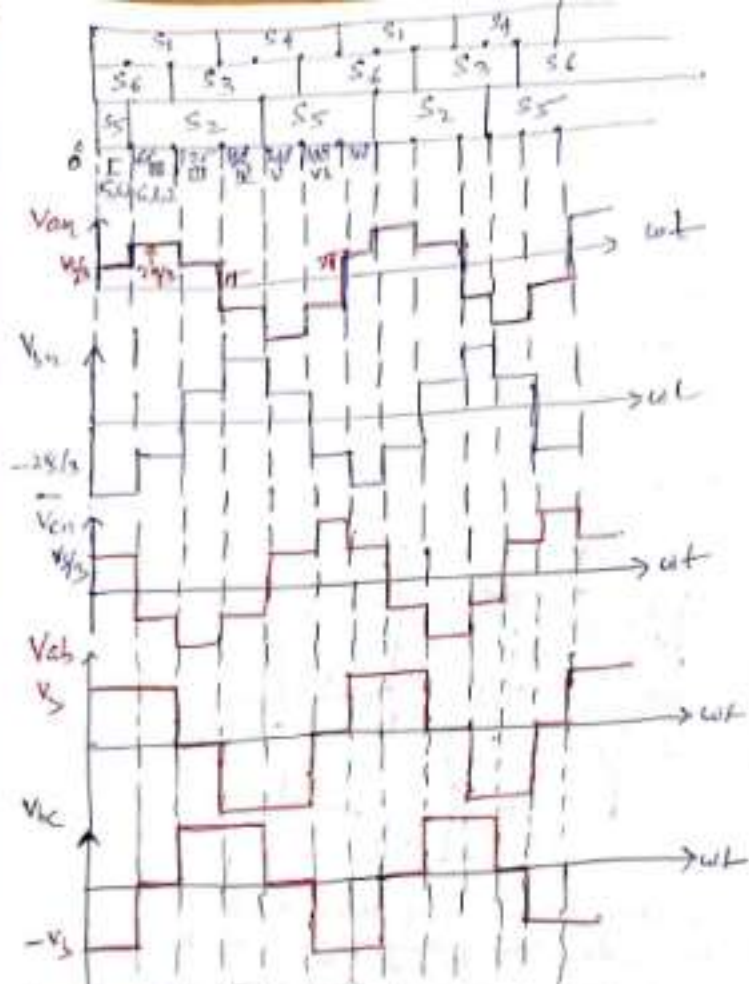
$$I = \frac{V_s \times 2}{3R} = \frac{2V_s}{3R}$$

$$V_{an} = \frac{V_s}{3} \times \frac{R}{R} = \frac{V_s}{3}$$

$$V_{cn} = \frac{V_s}{3}$$

$$V_{bn} = -\frac{2V_s}{3}$$

$$I_1 = \frac{2V_s \times R}{3R \times 2R} = \frac{V_s}{3R}$$



Mode II (6, 1, 2) thyristor conduct.

$$V_{an} = \frac{2V_s}{3} \quad V_{bn} = V_{cn} = -\frac{V_s}{3}$$

Mode III (1, 2, 3) thyristor conduct

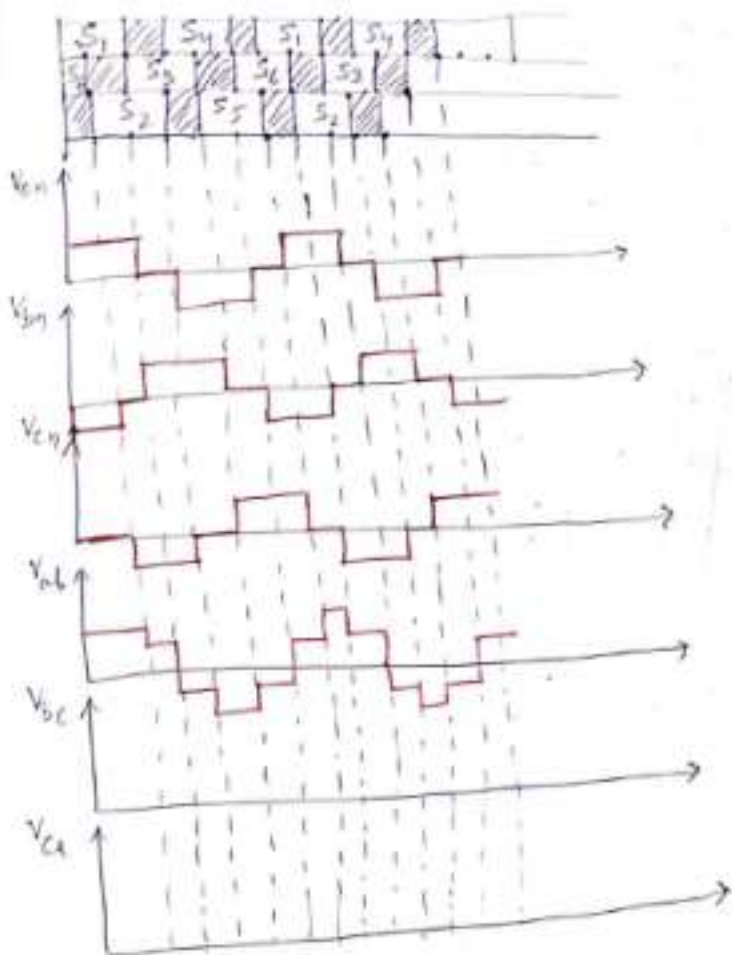
$$V_{an} = 0 \quad V_{bn} = \frac{V_s}{3} \quad V_{cn} = -\frac{2V_s}{3}$$

Rms value of line voltage  $V_L$  is  $V_L = \left[ \frac{1}{\pi} \int_0^{2\pi} V_s^2 d(\omega t) \right]^{1/2}$

$$= \sqrt{\frac{2}{3}} V_s = 0.8165 V_s$$

Rms value of phase voltage  $V_p = V_L / \sqrt{3} = \frac{\sqrt{2}}{\sqrt{3}} V_s = 0.8165 V_s$

$$V_{p1} = \frac{2V_s}{\sqrt{2}\pi} = 0.4502V_s = \frac{V_L}{\sqrt{3}}$$



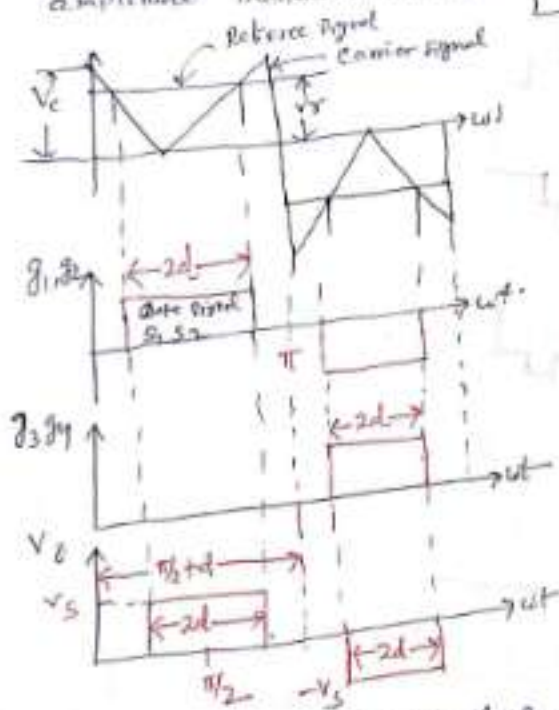
### Pulse width modulation control :-

Advantages :- (1) With this method, lower order harmonics can be eliminated or minimized along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimized.

Disadvantages :- The main disadvantage of this method is that if SCR are used, then these SCRs must possess low turn on and turn off time (inverter grade SCRs). As a result, PWM control with SCRs is expensive.

### Single pulse width Modulation:-

In this modulation, one voltage pulse in each half cycle is produced. The width of this pulse is varied to control the inverter output voltage. A rectangular reference signal of amplitude  $V_r$  is compared with triangular carrier wave of amplitude  $V_c$  in reference signal frequency determines the fundamental frequency of the output voltage. The ratio of  $V_r$  to  $V_c$  ( $\frac{V_r}{V_c}$ ) is the control variable and is called modulation index  $M$ . Thus amplitude modulation index  $M = \frac{V_r}{V_c}$



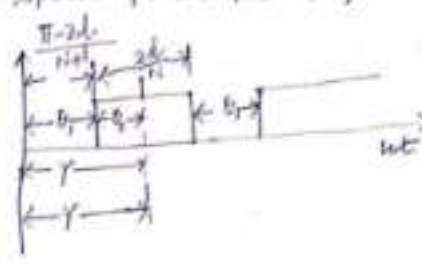
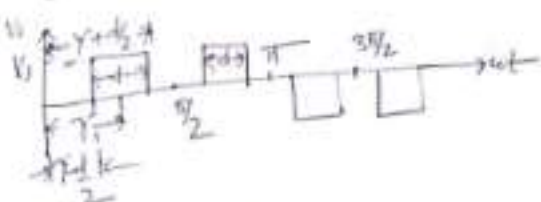
\* when  $V_r > V_c$ , gate signal of width  $2d$  are generated for switch  $S_1, S_2$  and  $S_3, S_4$ . When these switches are on modulated ac output voltage of amplitude  $V_s$  and width  $2d$  is generated.

\* The output voltage is controlled by varying the pulse width  $2d$

$$\text{The rms output voltage } V_{or} = \left[ \frac{V_s^2 \cdot 2d}{\pi} \right]^{1/2} = V_s \left[ \frac{2d}{\pi} \right]^{1/2}$$

## Multiple Pulse-width Modulation:-

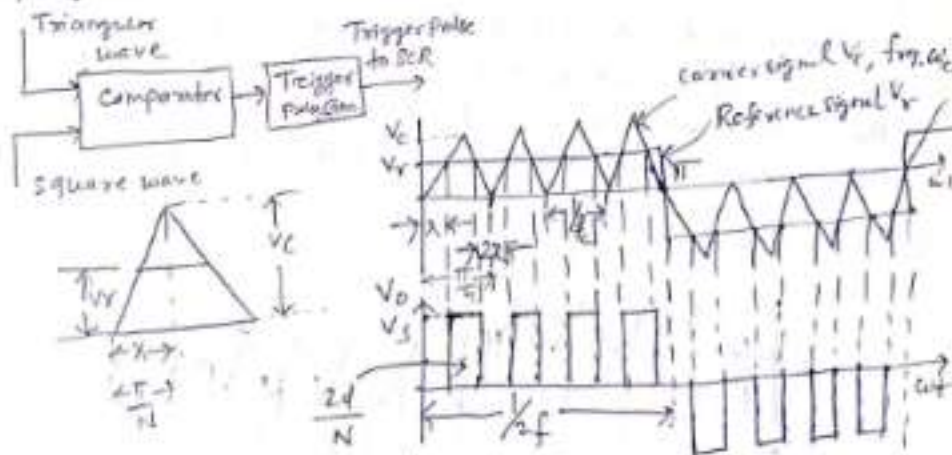
This method of pulse modulation is an extension of single-pulse modulation. In multiple pulse modulation (MPWM), several equidistant pulses per half cycle are used. For simplicity, the effect of varying two symmetrically spaced pulses per half cycle, is investigated here.



$$\gamma = \frac{\pi}{N} \quad \text{or} \quad d = \frac{2\pi}{N}$$

$$\gamma = \frac{\pi - 2d}{N+1} + \frac{2d}{2N} = \frac{\pi - 2d}{N+1} + \frac{d}{N}$$

\* More number of pulses per half cycle, the amplitude of lower order harmonics are reduced.



For triangular carrier wave, Pulse width =  $\frac{1}{f}$

For square reference wave, width of half cycle =  $\frac{1}{2f}$

$N = \text{Number of pulse per half cycle} = \frac{\text{width of half cycle of square wave}}{\text{width of triangular carrier wave}}$

$$M = \frac{V_r/2f}{1/f_c} = \frac{f_c}{2f} = \frac{V_c}{2V_r}$$

\* Pulse height of the reference or modulating signal can be controlled within the range of  $0 < V_r < V_c$  and pulse width  $2d/N$  varied in the range of  $0 < \frac{2d}{N} < \frac{\pi}{N}$

$$V_{out} = V_s \left[ \frac{2d}{\pi} \right]^{1/2}$$

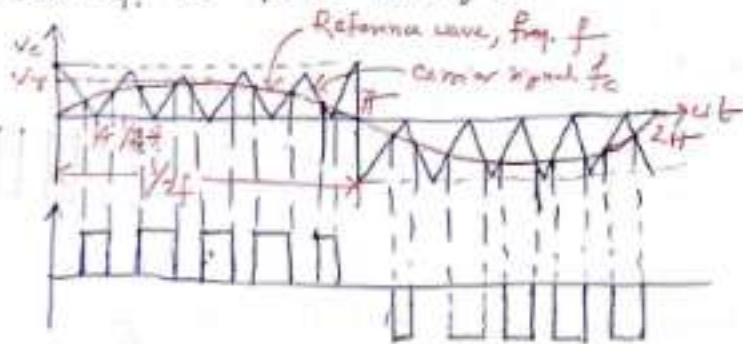
$$\frac{2d}{N} = \frac{\pi}{N} - 2x$$

$$\frac{V_s}{\pi/2N} = \frac{V_r}{x} \quad \text{or } x = \frac{\pi}{2N} \cdot \frac{V_r}{V_c}$$

$$\begin{aligned} \text{Pulse width is } \frac{2d}{N} &= \left( \frac{\pi}{N} - \frac{\pi}{N} \cdot \frac{V_r}{V_c} \right) \\ &= \left( 1 - \frac{V_r}{V_c} \right) \frac{\pi}{N} \end{aligned}$$

### Sinusoidal-pulse width modulation

In this method, several pulses per half cycle are used as in the case of multiple pulse width modulation. In MPWM, the pulse width is equal for all the pulses. But SPWM, the pulse width is a sinusoidal function of the angular position of the pulse in a cycle.



High frequency triangular carrier wave  $V_c$  is compared with a sinusoidal reference wave  $V_r = V_r \sin \omega t$  of the desired frequency. The intersection of  $V_c$  and  $V_r$  waves determines the switching instants and commutations of the modulated pulse.  $V_c$  is the peak value of triangular carrier wave and  $V_r$  that reference or modulating signal. The carrier and reference wave are mixed in a comparator. When sinusoidal wave has amplitude  $V_r$  higher than amplitude  $V_c$  of triangular wave, the comparator output is high, otherwise it is low. The comparator output is processed in a trigger pulse generator in such a manner that the output voltage wave of the inverter has a pulse width in agreement with the comparator output pulse width. Frequency of reference signal determines the inverter output frequency.

\* When triangular carrier wave has its peak coincident with zero of reference sinusoid, there are  $N = \frac{f_c}{2f}$  pulses per half cycle.

\* In case of zero of the triangular wave coincides with zero of reference sinusoid, there are  $(N-1)$  pulses per half cycle.  $\left(\frac{f_c}{2f} - 1\right)$  pulses per half cycle.

\* The ratio of  $\frac{V_r}{V_c}$  is called modulation index (MI) it controls the harmonic content of the output voltage waveform.

\* For  $M < 1$ , largest harmonic amplitude in the output voltage are associated with harmonics of the order  $\frac{f_c}{2f} \pm 1$  or  $2N \pm 1$ . By increasing the number of pulses per half cycle, the order of dominant harmonics frequency can be raised, which can be filtered out easily.

\* If  $N$  is increased, the order of significant harmonics increases and the filtering requirements are minimized.

† If  $\omega$  is greater than  $\omega_{c1}$ , lower order harmonics appear since  $\omega > \omega_{c1}$ , pulse width is no longer a sinusoidal function of the angular position of the pulse.

### Current source inverters (CSI)

In CSI, the input current is constant but adjustable. The amplitude of output current from CSI is independent of the load. The magnitude of output voltage and its waveform output from CSI is dependent upon the nature of load impedance.

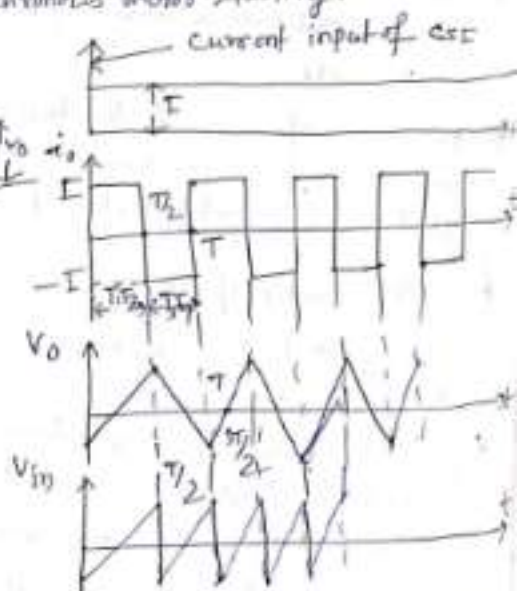
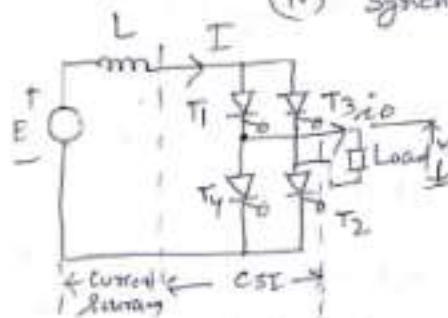
† A CSI converts the input dc current to an ac current at its output terminals.

Applications: (i) Speed control of ac motors

(ii) Induction heating

(iii) Lagging VAR compensation

(iv) Synchronous motor starting.



The source current of a voltage source  $E$  and large inductance  $L$  in series with it. The function of high-impedance inductor in series with voltage source is to maintain a constant current. When  $T_1$  and  $T_2$  is on, load current  $i_o$  is positive and

equal to  $I$ , when  $T_3$  and  $T_4$  are on load current  $i_o$  is negative and equal to  $-I$ . The output current  $i_o$  is a square wave of amplitude equal to dc input current  $I$ .

Assume that load consist of a capacitor  $C$ . It is known for a capacitor that

$$i_o = C \frac{dv_o}{dt}$$

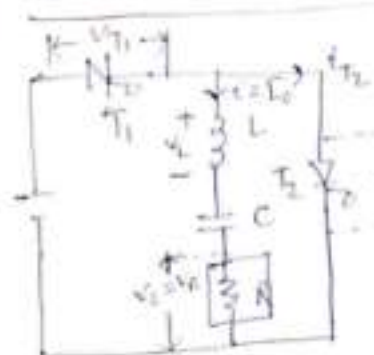
As  $i_o$  is constant, slope  $\frac{dv_o}{dt}$  must be constant over every half cycle. The slope from zero to  $T/2$  to  $T$ . The input voltage to the CSE  $V_{in} = V_o$  when  $T_1, T_2$  conduct and  $V_{in} = -V_o$  when  $T_3, T_4$  conduct.

\* The dc input current  $I$ , the input to the CSE is always unidirectional. If the average value of  $V_{in}$  is positive, power flows from source to load. In case average value of  $V_{in}$  is negative, power flows from load to source i.e. regeneration of power takes place.

\* Load commutation is possible when load PF is leading. For lagging PF load, forced commutation is essential.

Series inverter : - Inverters in which commutating components are permanently connected in series with the load are called series inverters. The series circuit so formed must be underdamped. As the current attains zero value due to the nature of the series circuit, series inverters are also classified as self-commutated inverters or load commutated inverters. These inverters operates at high frequencies (200 Hz to 100 kHz), the size of commutating component is small.

# Basic Series inverter



It consist of load resistance  $R$  in series with commutating components  $L$  and  $C$ . The value of  $L$  and  $C$  are so chosen, that the series RLC circuit forms an underdamped out. When thyristor  $T_1$  is turned  $V_{dc}$  on, with  $T_2$  off, current  $i_o$  starts building up in the  $RLC$  circuit. As the current is underdamped; the load current, after

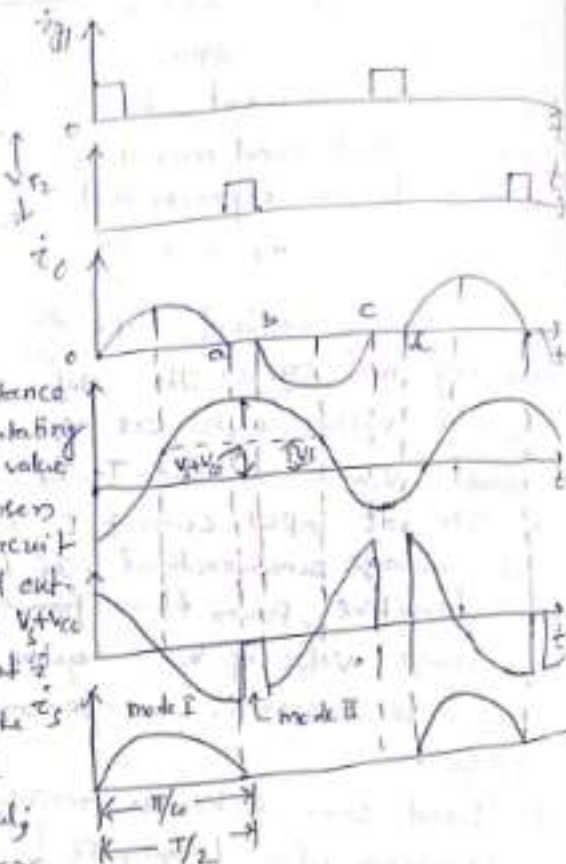
reaching some peak value, decays to zero at point a. At point a, as the load current tends to reverse, SCR  $T_1$  is turned off. After instant a, some minimum time  $t_{qmin}$  must elapse for  $T_1$  to regain its forward blocking capability. The minimum time is given by

$$t_{qmin} = \frac{\pi}{\omega} - \frac{\pi}{\omega_r} = \frac{1}{2} \left( \frac{1}{f} - \frac{1}{f_r} \right)$$

$\omega$  = output frequency in rad/sec

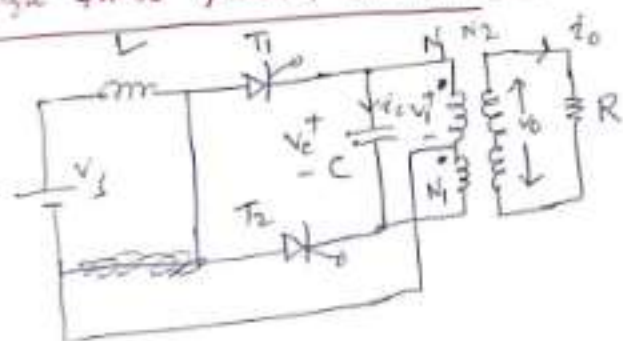
$\omega_r$  = circuit ringing frequency in rad/sec

Time interval between the instant  $T_1$  is turned off and the instant  $T_2$  is turned on is indicated by  $t_{off} = ab$ ,



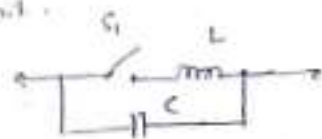
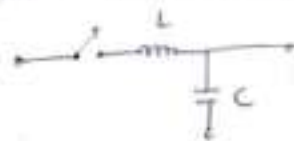
when  $T_{off} > t_{ymin}$ . After thyristor  $T_1$  has commutated capacitor attains positive polarity. Now when  $T_2$  is turned on at instant  $b$ , capacitor begins to discharge and the load current in the reverse direction build up to some peak negative value and then decay to zero at instant  $c$ .  $T_{off} = ab$ , or  $cd$  is called circuit turn-off time or dead zone time.

single phase parallel inverter:

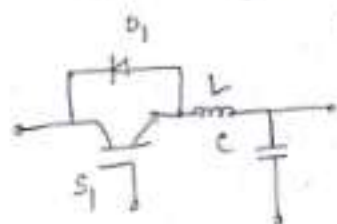
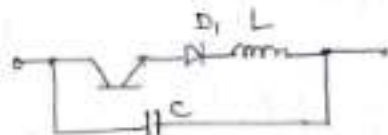


## Zero Current Switching Resonant Converters

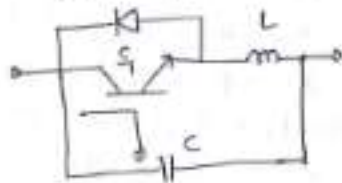
The switches of Zero-current Switching (ZCS) resonant converter turn-on and off at zero current. It is classified into two types L-type and  $\pi$ -types, the function of L ZCS is  $di/dt$  of the switch current, L and C constitute a series resonant circuit.



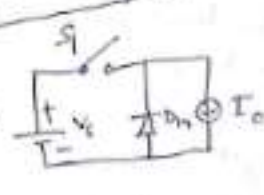
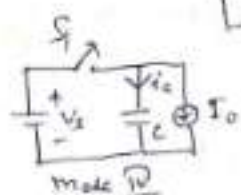
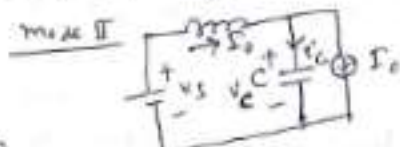
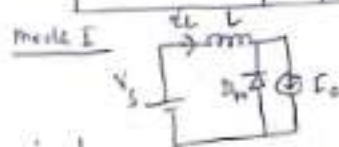
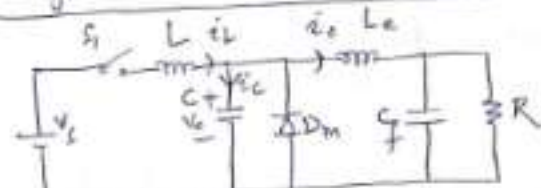
$\pi$ -type



Halfwave type D1



### L-type ZCS Resonant Converter



Mode I :- This mode of operation valid for  $0 \leq t \leq t_1$ . Switch  $S_1$  is turned on and diode  $D_m$  conducts. The inductor current  $i_L$  which rises linearly, is given by  $i_L = \frac{V_s}{L} t$ . This mode ends at  $t = t_1$  when  $i_L(t = t_1) = I_o$ ,  $t_1 = I_o L / V_s$

mode II This mode of operation is for  $0 \leq t \leq t_2$ . When switches  $S_1$  remain on, but diode  $D_1$  is off. The inductor current  $i_L$  is  $2V_s$  given by

$$i_L = I_{\text{in}} \sin \omega t + I_0$$

$$t_w = V_s \sqrt{L/C} \quad \omega = \frac{1}{\sqrt{LC}}$$

The capacitor voltage  $V_c$  is given by  $V_c = V_s (1 - \cos \omega t)$ . The peak current which occurs at  $t = \pi/2 \sqrt{LC}$  is  $I_p = I_{\text{in}} + I_0$

The peak capacitor voltage is  $V_{c(\text{pk})} = 2V_s$ . This mode ends at  $t = t_2$  when  $i_L(t = t_2) = I_0$  and  $V_c(t = t_2) = V_{c2} = 2V_s$

Therefore  $t_2 = \pi \sqrt{LC}$

mode III This mode is valid for  $0 \leq t \leq t_3$ . The inductor current that falls from  $I_0$  to zero is given by  $i_L = I_0 - I_{\text{in}} \sin \omega t$  and the capacitor voltage  $V_c = 2V_s \cos \omega t$ . This mode ends at  $t = t_3$  when  $i_L(t = t_3) = 0$  and  $V_c(t = t_3) = V_{c3}$

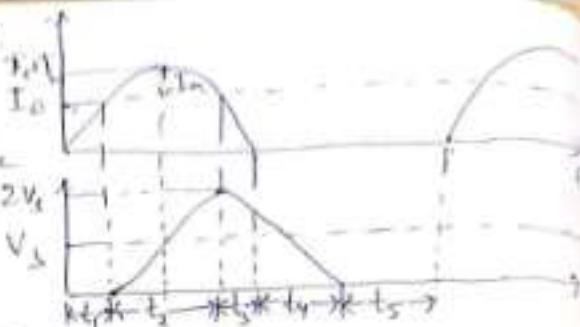
$$t_3 = \sqrt{LC} \sin^{-1} \left( \frac{I_0}{I_{\text{in}}} \right) \quad \text{where } x = I_0/I_{\text{in}} = \left( V_s/I_{\text{in}} \right) \sqrt{C/L}$$

mode IV This mode is valid for  $0 \leq t \leq t_4$ . The capacitor supplies the load current  $I_0$  and its voltage is given by

$$V_c = V_{c3} - \frac{I_0}{C} t$$

This mode ends at time  $t = t_4$  when  $V_c(t = t_4) = 0$ ,  $t_4 = V_{c3} C / I_0$

mode V This mode is valid for  $0 \leq t \leq t_5$ . When capacitor voltage tends to be negative, the diode  $D_1$  conducts. The load current  $I_0$  flows through diode  $D_1$ . This mode ends at time  $t = t_5$  when the switch  $S_1$  is turned on again and the cycle is repeated.  $t_5 = T - (t_1 + t_2 + t_3 + t_4)$



VSE

d.c source has small resistance.

- It has stiff d.c voltage source.
- Feedback: O/P voltage is affected by the load.
- It require feedback.

CSE

d.c source of high impedance. Stiff current source.

O/P current are not affected by load.

A CSE does not require feedback diode.

### Space Vector modulation :-

- It is a digital modulating technique where the objective is to generate PWM load line voltage.
- This is done in each sampling period by properly selecting the switch state of the inverter and calculation of the time period for each state.

⊗

$$u_a(t) + u_b(t) + u_c(t) = 0$$

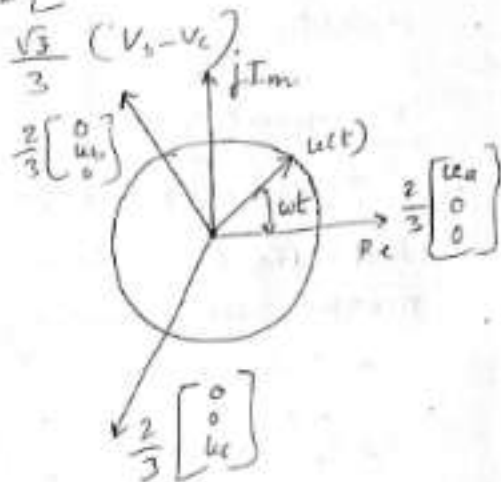
$$u(t) = \frac{2}{3} \left[ u_a + u_b e^{j\frac{2\pi}{3}} + u_c e^{-j\frac{2\pi}{3}} \right]$$

This three space vector can be transformed by two axis model.

$$\begin{bmatrix} u_x \\ u_y \end{bmatrix} = \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

$$u_x = \frac{2}{3} [V_a - 0.5(V_b + V_c)]$$

$$u_y = \frac{\sqrt{3}}{3} (V_b - V_c)$$



Space Vectors - The six thyristors will operate in a three phase bridge inverter. The six states thyristors are considering six switches. This switching states are represented by binary values:  $q_1, q_2, q_3, q_4, q_5, q_6$ .  
 $q_k = 1$  when switch is ON.  
 $q_k = 0$  when " is off.

Using transformation, the line voltage as the reference, the d-q components of the rms output voltage vector can be expressed as  $q_1, q_2, q_3$

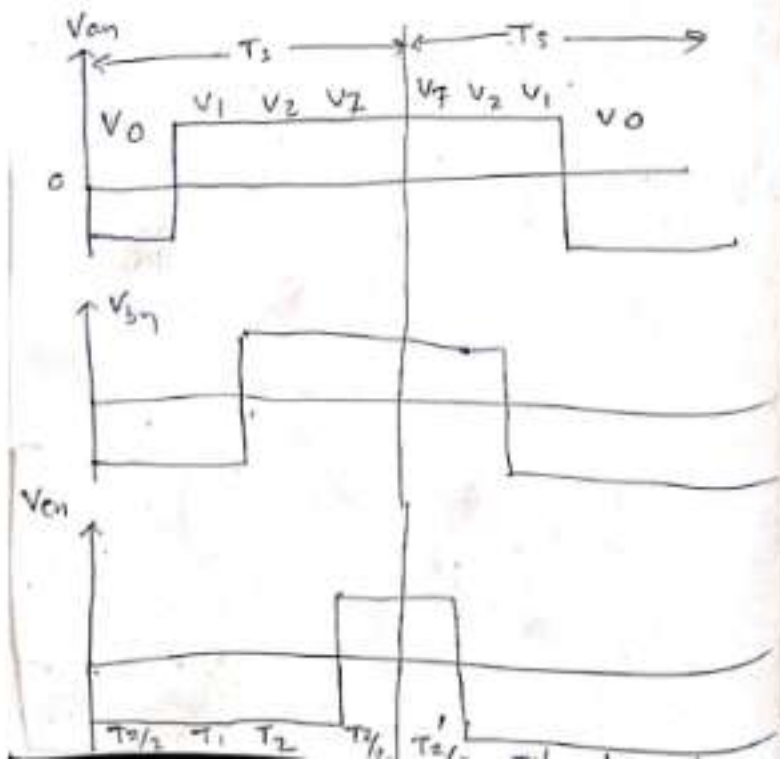
$$\begin{bmatrix} V_{Ld} \\ V_{Lq} \end{bmatrix} = \frac{2}{3} \sqrt{\frac{3}{2}} V_s \begin{pmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \begin{bmatrix} q_1 \\ q_2 \\ q_3 \end{bmatrix}$$

SV Switching:- The objective of SV switching is to obtain sinusoidal voltage.

SV sequence:-

The space vector sequence should ensure that the load line voltage have the quarter wave symmetry to reduce even harmonics.

- To reduce switching frequency, to arrange switching sequence.
- The switching sequence  $V_0, V_1, V_2, V_2, V_1, V_0$ .



The time interval  $T_2$  is from  $T_0$  to  $T_2$ .

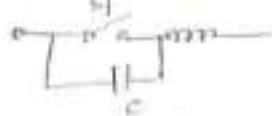
The three phase o/p voltage is obtained in two sampling period.

To minimize, uncharacteristic harmonic in SV modulation, the sampling period frequency is  $f_{s1}$  should be an integer multiple of 6,  $T \gg 6nT_c$ .  $n = 1, 2, 3$ .

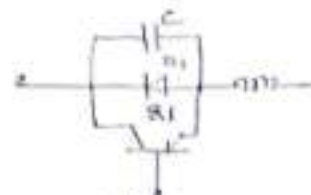
All six sectors should be equally used in one period for producing symmetrical o/p voltage.

### Zero voltage switching Resonant converter.

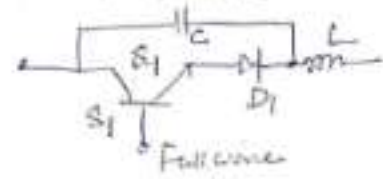
- ① The ZVS resonant converter turns on and turn off at zero voltage.
- ② The capacitor  $C$  is in parallel with switch  $S_1$  to form ZVS.
- ③ The internal switching capacitance  $C_j$  is added with the capacitance  $C$  and it effect the resonant frequency nearly no power loss.



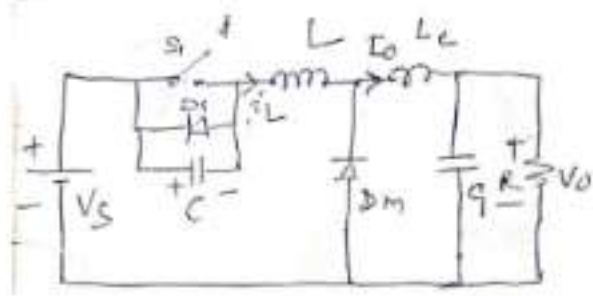
ZVS switch



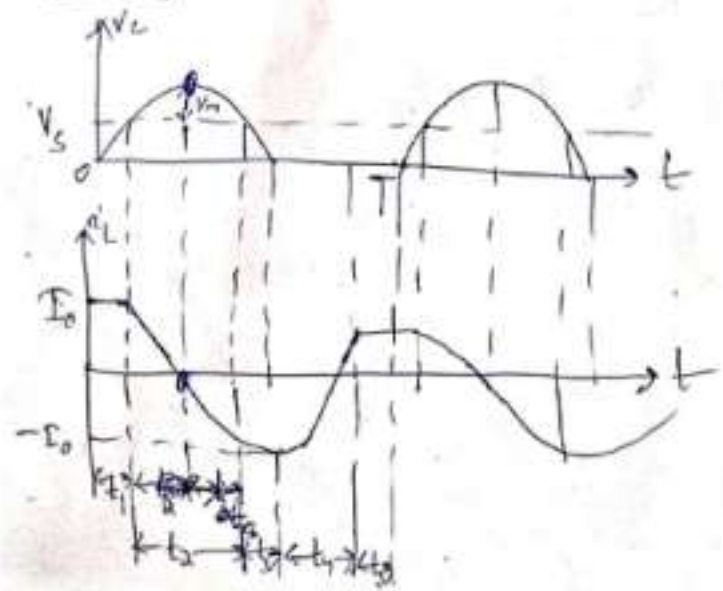
Half wave



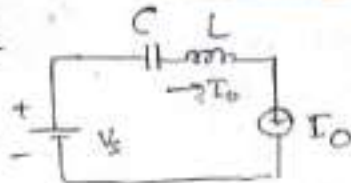
Full wave



problem



Mode I :-



This is valid for  $0 \leq t \leq t_1$ . The switch  $S_1$  and diode  $D_m$  are off. The capacitor is charged at a constant rate of  $I_0$ . Current  $I_0$ . The capacitor voltage  $V_c = \frac{I_0}{C} t$ . This mode ends at time  $t = t_1$ , when  $V_c = V_s$ . This  $t_1 = V_s C / I_0$ .

Mode II :- This mode is valid for  $0 \leq t \leq t_2$ . The switch  $S_1$  is still off, but diode  $D_m$  turns on. The capacitor voltage  $V_c$  is given by

$$V_c = V_m \sin \omega t + V_s$$

$V_m = I_0 \sqrt{L/C}$ . The peak switch voltage which occurs at  $t = \pi/2 \sqrt{L/C}$ .

$$V_{T(\text{peak})} = V_{S(\text{peak})} = I_0 \sqrt{L/C} + V_s$$

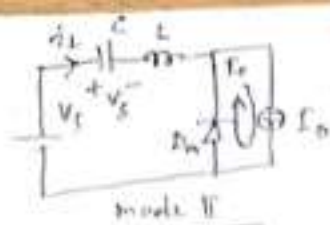
The inductor current  $i_L$  is given by

$$i_L = I_0 \cos \omega t$$

This mode ends at  $t = t_2$ ,  $V_c(t = t_2) = V_s$

$$i_L(t = t_2) = -I_0, \text{ therefore, } t_2 = \pi \sqrt{L/C}$$

Mode 3 :- This mode is valid for  $0 \leq t \leq t_3$ . The capacitor voltage that falls  $V_c$  to zero is given by  $V_c = V_s - V_m \sin \omega t$



The inductor current  $i_L$  is given by

$$-i_L = -I_o \cos \omega t$$

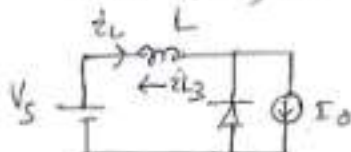
This mode ends at  $t = t_3$  when  $V_C(t=t_3) = 0$ ,

$$-i_L(t=t_3) = I_{L2} \text{ Thus}$$

$$t_3 = \sqrt{LC} \sin^{-1} x$$

$$\text{when } x = V_s / V_m = (V_s / I_o) \sqrt{\frac{C}{L}}$$

mode III



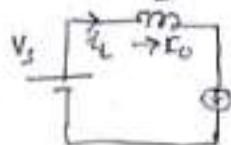
This mode is valid for  $0 \leq t \leq t_4$ . Switch  $S_1$  is turned on, and diode  $D_m$  remain on.

The inductor current, which rises linearly from  $I_{L2}$  to  $I_o$  is given by

$$i_L = i_{L2} + \frac{V_s}{L} t$$

This mode ends at time  $t = t_4$  when  $i_L = 0$ . Thus  $t_4 = (I_o - I_{L2}) (L/V_s)$ . Note that  $I_{L2}$  is a negative value.

mode IV :-



This mode is valid for  $0 \leq t \leq t_5$ . Switch  $S_1$  is on, but  $D_m$  is off. The load current  $I_o$  flows through the switch. This mode ends at time  $t_5$  when switch  $S_1$  is turned off again and II

cycle is repeated.  $t_s = T - (t_1 + t_2 + t_3 + t_4)$

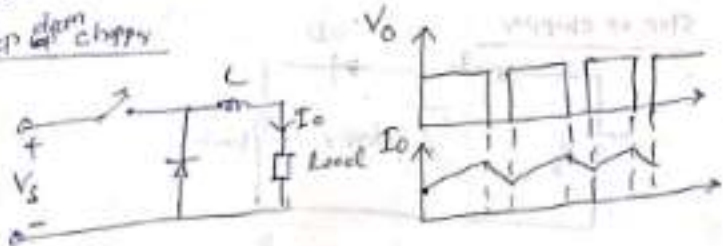
## **MODULE- V**

A chopper is a static device that converts fixed d.c. input voltage to variable d.c. output voltage. A chopper may be thought of as d.c. equivalent of an a.c. transformer.

- Applications:-
- (a) trolley car.
  - (b) motor drives.
  - (c) speed brakes.
  - (d) mine hoists.

The power semiconductor devices used for a chopper ckt can be Power BJT, Power MOSFET, GTO or free commutated thyristors.

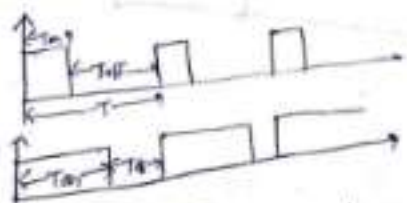
Step down chopper



$V_o = \alpha V_s$   
 $\alpha = \text{duty cycle}$

(a) Constant frequency chopping

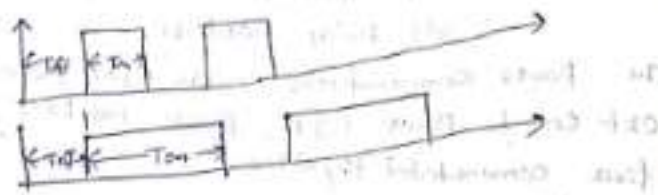
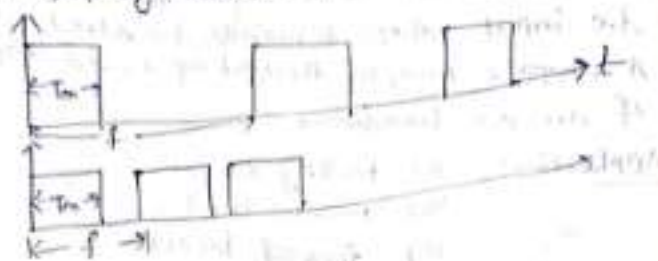
In this scheme, the on time  $T_{on}$  is varied, but chopping frequency is kept constant. Variation of  $T_{on}$  means adjustment of pulse width. Such scheme is also called pulse-width-modulation scheme.



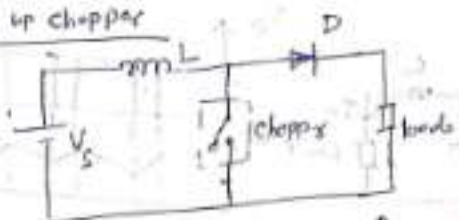
(b) Variable frequency chopping:-

In this scheme, the chopping frequency is varied and either on time  $T_{on}$  is kept constant.

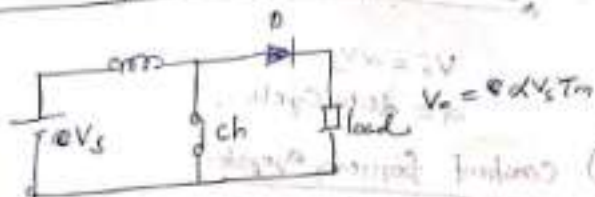
(c) off time  $T_{off}$  is constant. The method is also called frequency modulation scheme.



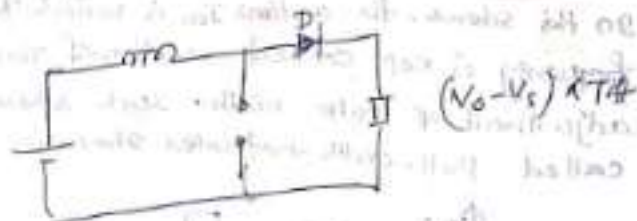
Step up chopper



Mode I



Mode II

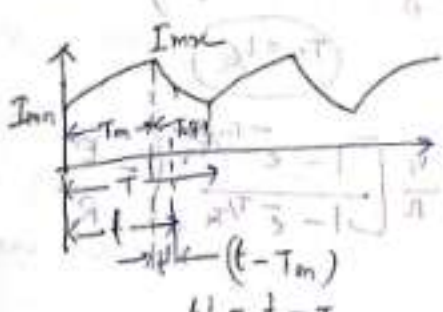
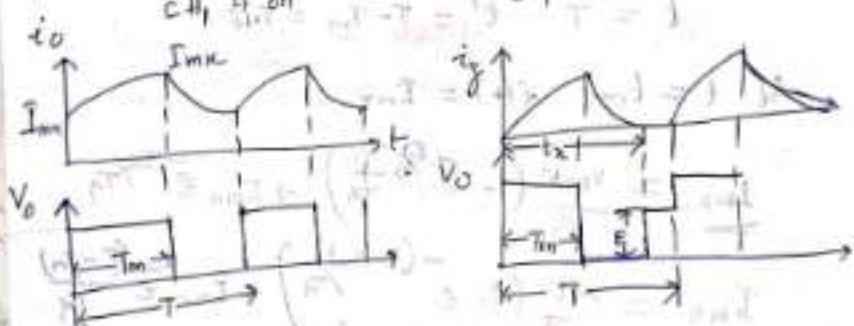
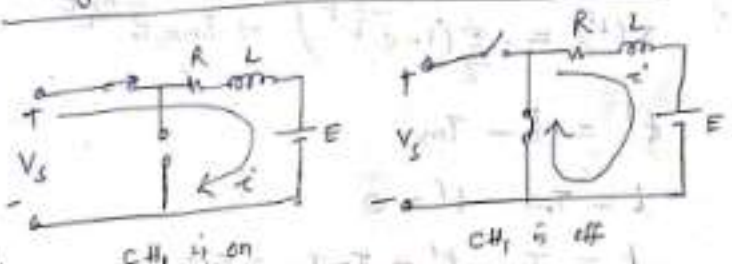


for a constant output voltage, the chopping frequency must be increased. In this scheme, the chopping frequency is varied with the output voltage.

- (a) Average output voltage =  $\alpha V_s$
- (b) average output current =  $\frac{\alpha V_s}{R}$
- (c) RMS value of the output voltage =  $\sqrt{\alpha} V_s$
- (d) Average thyristor current =  $\frac{\alpha V_s}{R}$
- (e) RMS thyristor current =  $\frac{\sqrt{\alpha} V_s}{R}$
- (f) effective input resistance of the chopper  

$$= \frac{\text{d.c. source voltage}}{\text{average source current}} = \frac{V_s \cdot R}{\alpha V_s} = \frac{R}{\alpha}$$

Steady State <sup>time domain</sup> analysis of Type A chopper



$$V_s = Ri + L \frac{di}{dt} + E \quad 0 \leq t < T_{on} \quad (1)$$

$$0 = Ri + L \frac{di}{dt} + E \quad T_{on} < t < T_{off} \quad (2)$$

$$Ri(t) + L \left[ \frac{di(t)}{dt} - I_{min} \right] = \frac{V_s - E}{s} \quad (1')$$

$$Ri(t) + L \left[ s di(t) - I_{min} \right] = -\frac{E}{s} \quad (2')$$

$$i(t) = \frac{V_s - E}{s(R + Ls)} + \frac{LI_{min}}{R + Ls} = \frac{V_s - E/Ls}{s(R/L + 1)} + \frac{I_{min}}{s(1 + \tau s)}$$

$$i(t) = \frac{V_s - E}{R} (1 - e^{-t/\tau}) + I_{min} e^{-t/\tau}$$

$$i'(t) = -\frac{E}{R} (1 - e^{-t'/\tau}) + I_{min} e^{-t'/\tau}$$

$$t' = t - T_{on}$$

$$t = T_{on} \quad t' = 0$$

$$t = T \quad t' = T - T_{on} = T_{off}$$

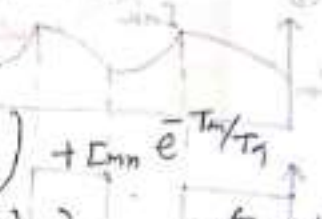
At  $t = t_{on}$   $i(t) = I_{min}$

$$I_{min} = \frac{V_s - E}{R} (1 - e^{-T_{on}/\tau}) + I_{min} e^{-T_{on}/\tau}$$

$$I_{min} = \frac{-E}{R} (1 - e^{-(T - T_{on})/\tau}) + I_{min} e^{-\frac{(T - T_{on})}{\tau}}$$

$$\tau = L/R$$

$$I_{min} = \frac{V_s}{R} \left[ \frac{1 - e^{-T_{on}/\tau}}{1 - e^{-T/\tau}} \right] - \frac{E}{R}$$

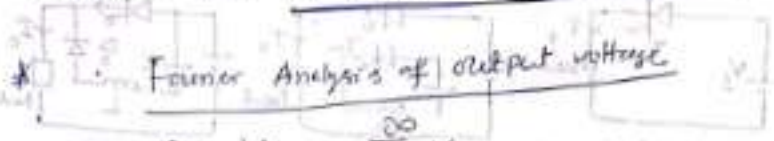


$$I_{min} = \frac{V_s}{R} \left[ \frac{e^{-T_d/T_a} - 1}{e^{T/T_a} - 1} \right] - \frac{E}{R}$$

Per unit ripple current =  $\frac{I_{max} - I_{min}}{V_s/R}$  ✓

∴ It's value is maximum when  $\alpha = 0.5$  ✓

As  $L$  increases  $T_d = L/R$  increases and  $T_a$  decreases and per ripple current decreases.



Fourier Analysis of output voltage

$$V = V_0 + \sum_{n=1}^{\infty} V_n$$

$V_n$  = value of  $n$ th harmonic voltage

$$= \frac{2V_s}{n\pi} \sin n\pi\alpha \cdot \sin(n\omega t + \theta_n)$$

$$V_0 = \alpha V_s, \quad \alpha = T_d/T \quad \theta_n = \tan^{-1} \frac{\sin 2n\pi\alpha}{1 - \cos 2n\pi\alpha}$$

The maximum value of  $n$ th harmonic occurs when  $\sin n\pi\alpha = 1$  and its value is

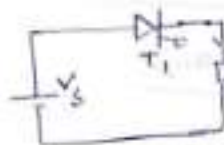
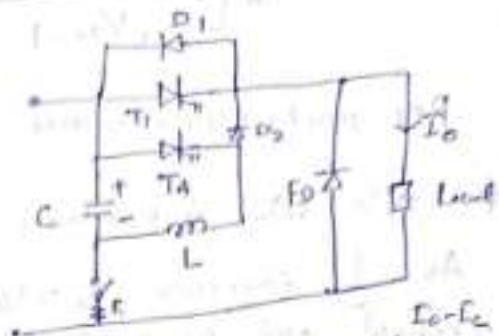
$$\frac{2V_s}{n\pi} = \frac{0.636 V_s}{n} \text{ volts.}$$

Rms value is  $\frac{2V_s}{n\pi\sqrt{2}} = \frac{0.45 V_s}{n}$  volts.

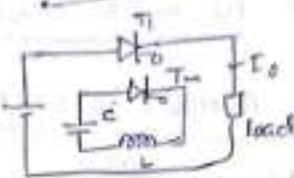
$$V_{R_{eff}} = V_s \sqrt{\alpha - \alpha^2}$$

∴ The effective value of the output voltage is  $V_s \sqrt{\alpha - \alpha^2}$ .  
 The effective value of the output current is  $I_o = I_0 \sqrt{\alpha - \alpha^2}$ .  
 The effective value of the output power is  $P_o = I_o^2 R$ .

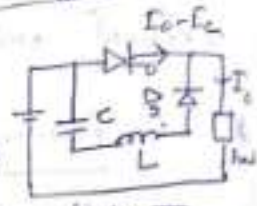
# Current Commutated Chopper :-



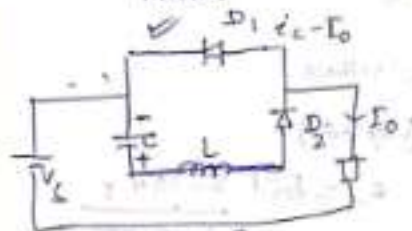
mode I



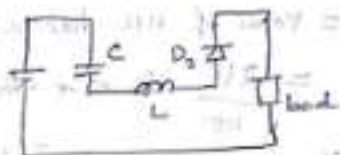
mode II



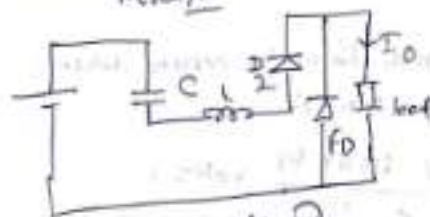
mode III



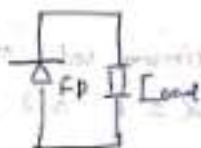
mode IV



mode V



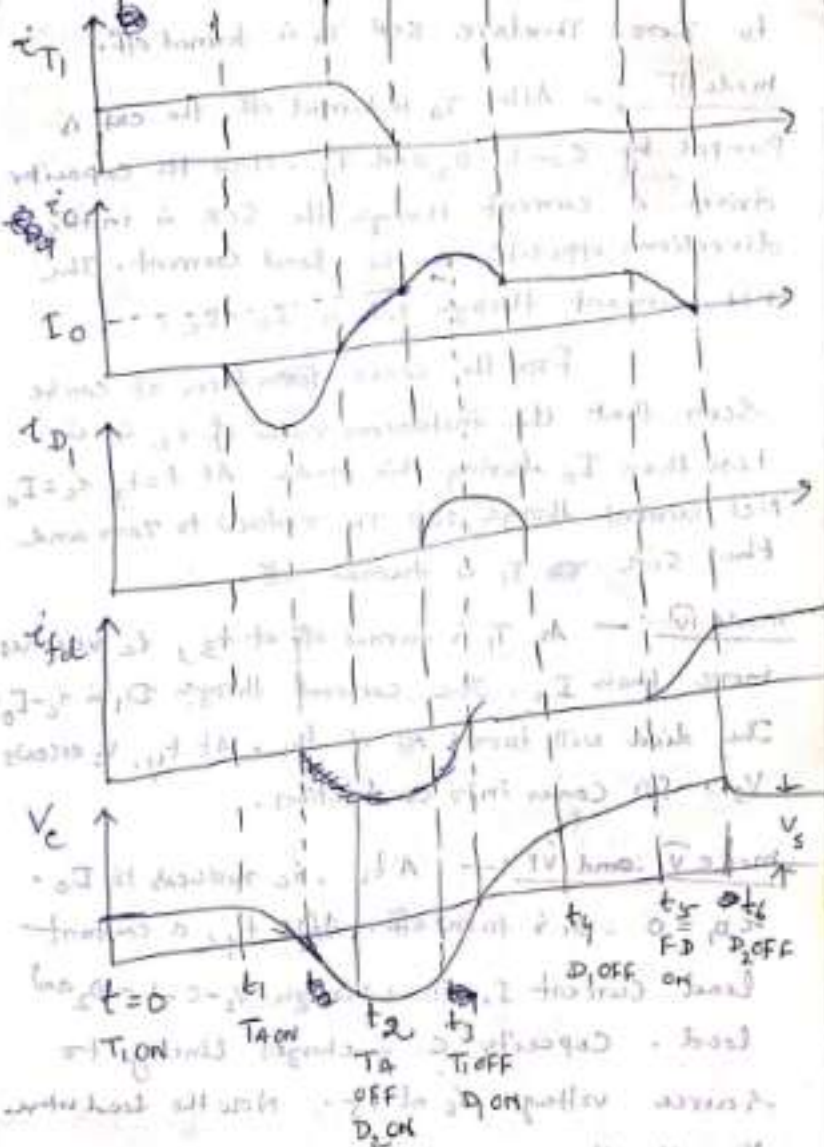
mode VI



mode VII

~~Part 1~~ First of all, capacitor C is charged to a voltage  $V_s$  through Resistance R.

mode I :- The main thyristor  $T_1$  is fired at  $t=0$  so that load voltage  $V_o = V_s$  and load current  $i_o = I_o$  upto  $t=t_1$ . With turning on the  $T_1$  commutation circuitry remains inactive.



mode II :- At time  $t = t_1$ , auxiliary thyristor  $T_2$  is triggered to commutate the main thyristor  $T_1$ . There are two current paths. Load current  $I_o$  flows through  $T_1$  &  $V_s$ . Rigging current flows through  $T_2$  &  $V_s$ . Rigging stops after half cycle. By the end of this rigging capacity polarity will reverse and current will

to zero. Therefore SCR  $T_1$  is turned off.

Mode III : - After  $T_1$  is turned off, the circuit is pumped by  $C, L, D_2$  and  $T_2$ . Now the capacitor drives a current through the SCR in the direction opposite to the load current. The net current through SCR is  $I_0 - I_c$ .

From the wave form it can be seen that the instantaneous value of  $i_c$  is less than  $I_0$  during this mode. At  $t = t_3$ ,  $i_c = I_0$ . Net current through SCR  $T_2$  reduced to zero and the SCR  $T_2$  is turned off.

Mode IV : - As  $T_2$  is turned off at  $t_3$ ,  $i_c$  becomes more than  $I_0$ . The current through  $D_1$  is  $i_c - I_0$ . The diode will turn off at  $t_4$ . At  $t_4$ ,  $V_c$  exceeds  $V_s$ . F.D. comes into conduction.

Mode V and VI : - At  $t_4$ ,  $i_c$  reduces to  $I_0$ .  $i_{D_1} = 0$ .  $D_1$  is turned off. After  $t_4$ , a constant load current  $I_0$  flows through  $V_s - C - L - D_2$  and load. Capacitor  $C$  is charged linearly to source voltage  $V_s$  at  $t_5$ . Now the load voltage  $V_0 = V_s - V_c$ .

Mode VII : - At  $t_5$ , capacitor is actually overcharged to voltage somewhat more than source voltage  $V_s$ . Therefore F.D. set forward biased. Load voltage  $V_0 = 0$  at  $t_5$ . At  $t_6$ ,  $i_c$  is that F.D. is conducting. F.D. then behaves as

After  $t_2$  only FD will conduct.

Designing:  $V_s \sqrt{\frac{C}{L}} \sin \omega t = I_{cp} \sin \omega t$

$$V_s \sqrt{\frac{C}{L}} \sin \omega t = I_{cp} \sin \omega t$$

$$I_{cp} = V_s \sqrt{\frac{C}{L}} > I_o$$

$$V_s \sqrt{\frac{C}{L}} = \alpha I_o$$

$$\alpha = \frac{I_{cp}}{I_o}$$

$$\omega t_c = \pi - 2\theta_1$$

$$I_{cp} \sin \theta_1 = I_o$$

$$\theta_1 = \sin^{-1} \left( \frac{I_o}{I_{cp}} \right) = \sin^{-1} \left( \frac{1}{\alpha} \right)$$

$$t_c = \frac{1}{\omega_o} (\pi - 2\theta_1)$$

$$t_c = \frac{1}{\omega_o} \left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right]$$

$$t_c = \left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right] \sqrt{LC}$$

$$\sqrt{C} = \frac{t_c}{\left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right] \sqrt{L}}$$

$$\frac{1}{C} = \frac{\omega_o^2 L t_c^2}{\left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right]^2}$$

$$\omega_o = \frac{1}{\sqrt{LC}}$$

$$\frac{1}{C} = \frac{L t_c^2}{\left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right]^2}$$

$$C = \frac{\left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right]^2}{L t_c^2}$$

$$C = \frac{\left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right]^2}{\omega_o^2 L t_c^2}$$

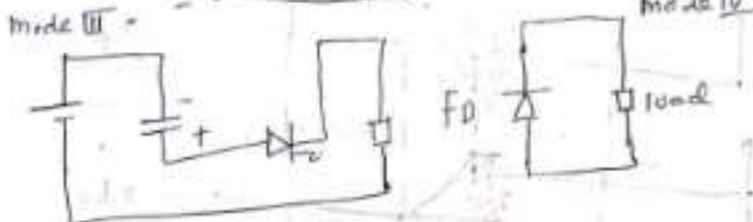
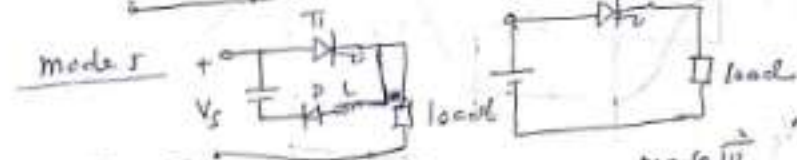
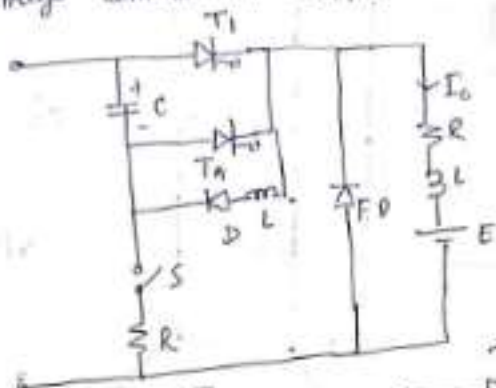
$$\omega_o = \frac{\left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right]}{L t_c \sqrt{C}}$$

2) Turnoff time for main SCR  $(t_4 - t_3) = \left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right] \sqrt{LC}$

3) Turnoff time for auxiliary thyristor  $(t_1 - t_2) = \left[ \pi - 2 \sin^{-1} \left( \frac{1}{\alpha} \right) \right] \sqrt{LC}$

# Chopper

① voltage commutated chopper



Design

$$i_c = C \frac{dv}{dt}$$

$$I_c = C \frac{V_s}{t_c}$$

$$C = \frac{t_c \cdot I_0}{V_s}$$

$$I_{cp} \leq I_0 \quad \text{or} \quad V_s \sqrt{\frac{C}{L}} \leq I_0$$

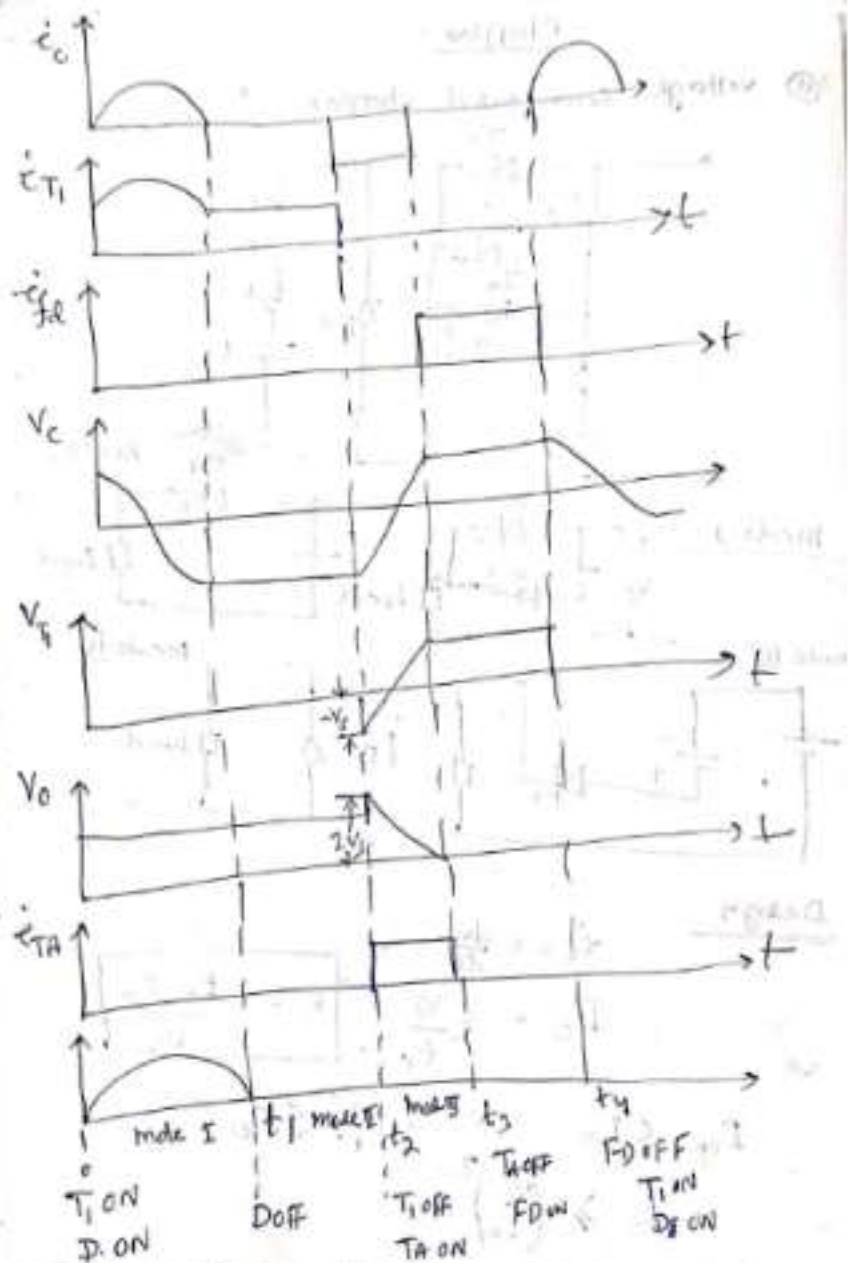
$$L \geq \left( \frac{V_s}{I_0} \right)^2 C$$

∴ circuit turn off time for auxiliary Thyristor =  $\frac{1}{2} \sqrt{LC}$

∴ Peak current through  $T_1$  is given by

$$I_{T1} = I_0 + V_s \sqrt{\frac{C}{L}}$$

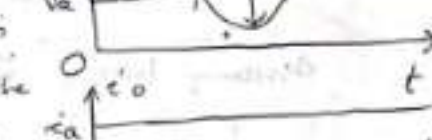
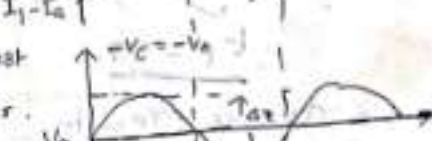
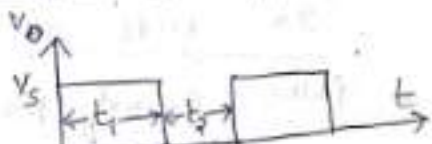
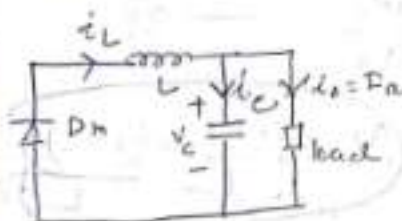
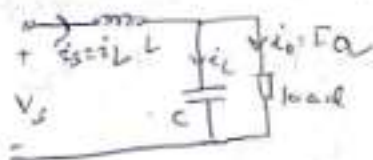
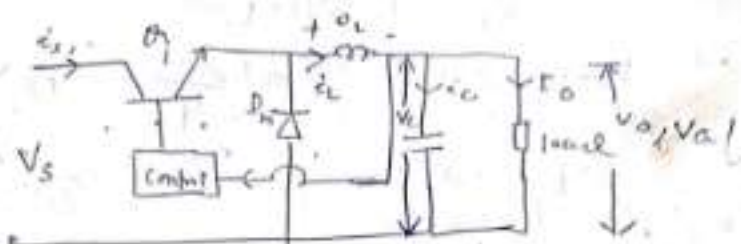
∴ Peak current through  $T_A = I_0$



Peak diode current  $= V_s \sqrt{\frac{C}{L}}$   
 effective on period  $T_{on} = T_{on} + \frac{2V_s C}{\omega_0}$

$T_{on} = t_1 - t_4$

# Buck Regulator :-



In buck regulator, average o/p voltage  $V_o$ , is less than  $I_1 - I_2$  the input voltage. It is just like a step down chopper.

mode 1 :- When transistor is switched on at  $t=0$ . The input current will rise through filter inductor  $L$ , filter capacitor  $C$ , and load resistor  $R$ .

mode 2 when the transistor  $Q_1$  is off at  $t_1$ , the freewheeling diode conducts. The energy trapped stored in inductor will flow through  $L$ ,  $C$ , and diode  $D_n$ .

The voltage across inductor L is, in general

$$e_L = L di/dt \quad \checkmark$$

$$V_s - V_a = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1} \quad \text{--- (1) } \checkmark$$

$$t_1 = \frac{\Delta I L}{V_s - V_a} \quad \text{--- (2)}$$

In mode 2: The inductor current falls linearly from  $I_2$  to  $I_1$  in time  $t_2$

$$-V_a = -L \frac{\Delta I}{t_2}$$

$$t_2 = \frac{\Delta I L}{V_a} \quad \text{--- (3)}$$

$$\begin{aligned} -L \frac{di}{dt} + V_a - V_s &= 0 \\ -L \frac{di}{dt} &= V_s - V_a \\ L \frac{di}{dt} &= V_a - V_s \end{aligned}$$

$$V_s - V_a = L \frac{\Delta I}{t_1}$$

$$\Delta I = \frac{V_a t_2}{L} = \frac{(V_s - V_a) t_2}{L}$$

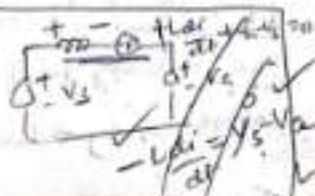
$$t_1 = kT$$

$$t_2 = (1-k)T$$

average of voltage  $V_a = V_s \frac{t_1}{T} = kV_s \quad \checkmark$

Assuming lossless  $V_s I_s = V_a I_a = kV_s I_a$   
 $I_s = kI_a \quad \checkmark$

$$T = \frac{1}{f} = t_1 + t_2 = \frac{L \Delta I}{V_s - V_a} + \frac{\Delta I L}{V_a}$$



$$= \frac{\Delta I L V_s}{V_a (V_s - V_a)}$$

Peak to peak ripple current

$$\Delta I = \frac{V_a (V_s - V_a)}{f L V_s}$$

0-21

10-22

$$\Delta I = \frac{V_s k (1-k)}{f L}$$

$$i_L = i_c + i_o$$

$$\Delta i_L = \Delta i_c$$

If we assume that load ripple current  $i_o$  is small, so the average capacitor current, which flows into

for  $t_{1/2} + t_{2/2} = T/2$  is

$$I_c = \frac{\Delta I}{4}$$

$$V_c = \frac{1}{C} \int i_c dt + V_c(t) \text{ (at } t=0)$$

$$\Delta V_c = V_c$$

Peak to peak ripple voltage of the capacitor is

$i_c = \frac{1}{2} \Delta I$   
 $\Delta I \ll I$

$$\Delta V_c = V_c - V_c(t=0) = \frac{1}{C} \int_0^{T/2} \frac{\Delta I}{4} dt$$

$$= \frac{\Delta I T}{8C} = \frac{\Delta I}{8fC}$$

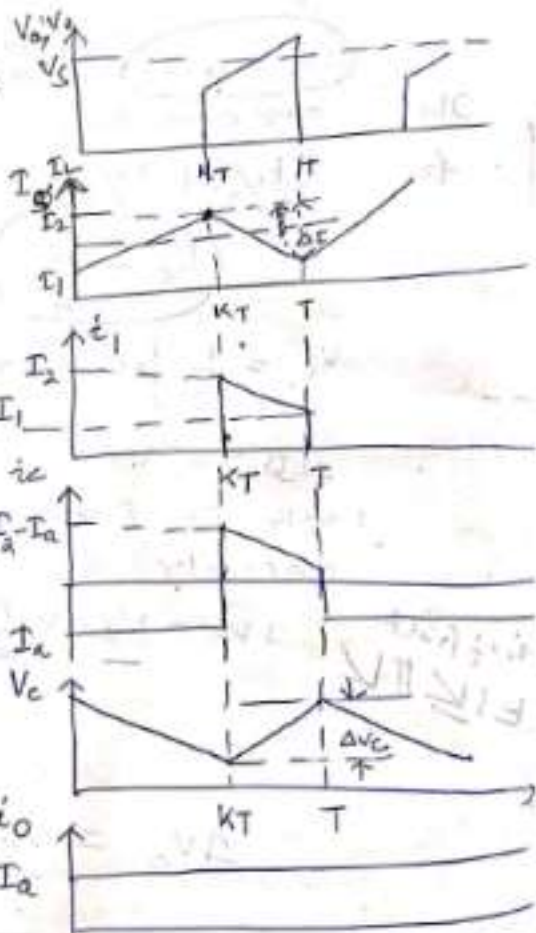
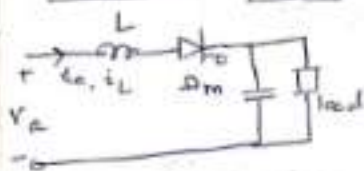
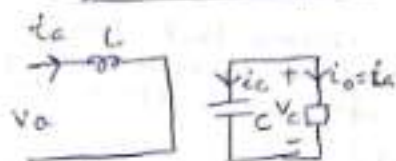
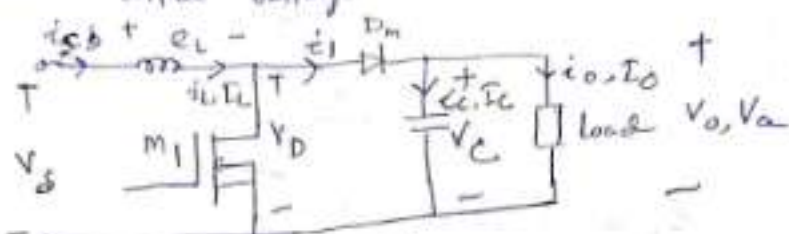
$$\Delta V_c = \frac{V_a (V_s - V_a)}{8 L C f^2 V_s}$$

$\frac{1}{2} \Delta I$

$$\Delta V_c = \frac{V_s k (1-k)}{8 L C f^2}$$

# Boost Regulator :-

↳ In this regulator output voltage is greater than input voltage.



*(Faint handwritten text, possibly a signature or date)*

mode I

When transistor  $M_1$  is switched on at  $t=0$ . The input current, which rises, flows through inductor  $L$  and transistor  $M_1$ .

mode II - when transistor  $M_1$  is switched off

at  $t=t_1$ . The current flows through the ~~transistor~~ inductor  $L$ ,  $C$ , Load and diode  $D_m$ . The energy stored in inductor  $L$  is transferred to load.

$$V_s = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1}$$

$$t_1 = L \frac{\Delta I}{V_s}$$

Inductor current falls linearly from  $I_2$  to  $I_1$  in time  $t_2$ .

$$V_s - V_a = -L \frac{\Delta I}{t_2}$$

$$t_2 = \frac{\Delta I L}{V_a - V_s}$$

$$\Delta I = \frac{V_s t_1}{L} = \frac{(V_a - V_s) t_2}{L}$$

$$t_1 = kT \quad t_2 = (1-k)T$$

$$V_a = V_s \frac{T}{t_2} = \frac{V_s}{1-k}$$

Assuming a lossless cut

$$V_s I_s = V_a I_a = V_s I_a / (1-k)$$

Average output current is  $I_s = \frac{I_a}{1-k}$

Switching period  $T$  can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I L}{V_s} + \frac{\Delta I L}{V_a - V_s} = \frac{\Delta I L V_a}{V_s (V_a - V_s)}$$

this gives the peak to peak ripple current

$$\Delta I = \frac{V_c (V_a - V_c)}{f L V_a}$$

$$\Delta I = \frac{V_c K}{f L}$$

When transistor is on, the capacitor supplies the load current for  $t = t_1$ . The average capacitor current during time  $t_1$  is  $I_c = I_a$  and peak to peak ripple voltage of the capacitor is

$$\Delta V_c = V_c - V_c(t=0) = \frac{1}{C} \int_0^{t_1} I_c dt = \frac{1}{C} \int_0^{t_1} I_a dt = \frac{I_a t_1}{C}$$

$$\Delta V_c = \frac{I_a (V_a - V_c)}{V_a f C} \quad \left[ \because t_1 = \frac{V_c - V_c}{V_a f} \right]$$

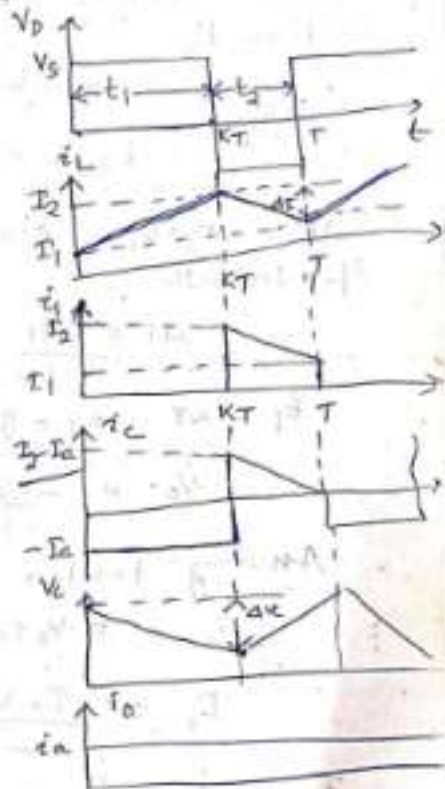
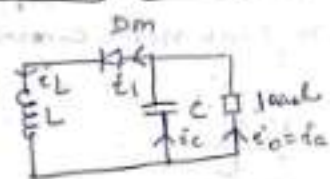
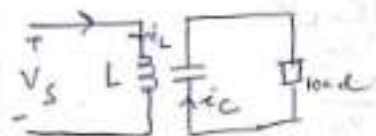
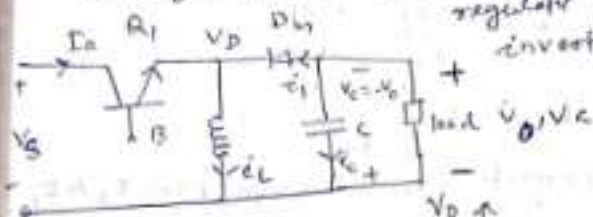
$$\Delta V_c = \frac{I_a K}{f C}$$

~~Power~~ ~~Power~~ ~~Power~~

### Buck-Boost Regulators: -

A buck-boost regulator provides an output voltage which may be less than or greater than the input voltage hence the name "buck-boost". The o/p voltage

Polarity is opposite to that of the input voltage. This regulator is known as inverting regulator.



The circuit operation can be divided into two modes. During mode 1, transistor  $Q_1$  is turned on and diode  $D_1$  is reverse biased.

During mode 2, transistor  $Q_1$  is switched off and the current which was flowing through inductor  $L$  would be transferred to the load and

inductor current would fall until transistor  $Q_1$  is switched on again in the next cycle.

Assuming that the inductor current rises linearly from  $I_1$  to  $I_2$  in time  $t_1$ ,

$$V_s = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1}$$

$$t_1 = \frac{\Delta I L}{V_s} \checkmark$$

Inductor current falls linearly from  $I_2$  to  $I_1$  in time  $t_2$ .

$$V_a = -L \frac{\Delta I}{t_2} \checkmark$$

$$t_2 = -\frac{\Delta I L}{V_a}$$

$\Delta I = I_2 - I_1$  = peak to peak ripple current of inductor.

$$\Delta I = \frac{V_s t_1}{L} = -\frac{V_a t_2}{L}$$

$$t_1 = kT \quad t_2 = (1-k)T$$

$$V_a = -\frac{V_s k}{1-k}$$

Assuming lossless  $V_s I_s = -V_a I_a$   
 $= V_s I_a k / (1-k)$

$$I_s = \frac{I_a k}{1-k}$$

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I L}{V_s} - \frac{\Delta I L}{V_a}$$

$$= \frac{\Delta I L (V_a - V_s)}{V_s V_a}$$

$$\Delta I = \frac{V_s V_a}{f L (V_a - V_s)}$$

$$\Delta C = \frac{V_a k}{fL}$$

$$\Delta V_c = \frac{1}{C} \int_0^{t_1} I_c dt = \frac{1}{C} \int_0^{t_1} I_a dt$$

$$= \frac{I_a t_1}{C}$$

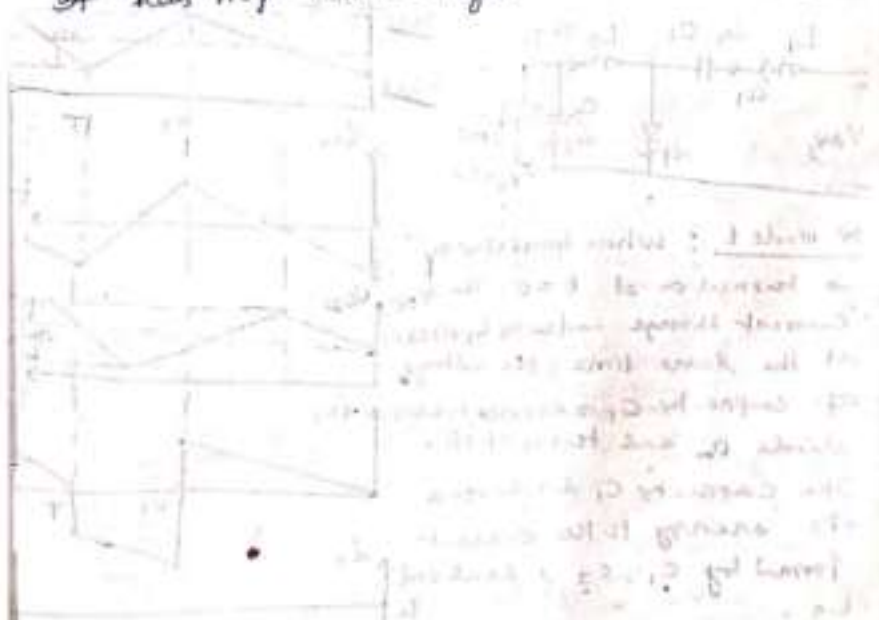
$$t_1 = \frac{V_a}{(V_a - V_s) f}$$

$$\Delta V_c = \frac{I_a V_a}{(V_a - V_s) f C}$$

$$\Delta V_c = \frac{I_a k}{f C}$$

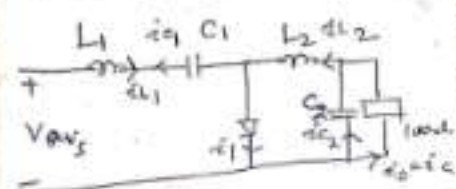
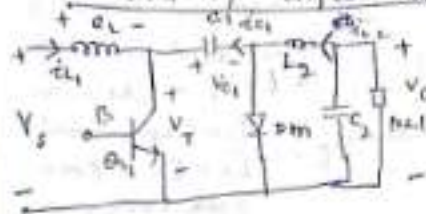
When transistor  $a_1$  is on, the filter capacitor supplies the load current for  $t = t_1$ . The average discharging current  $I_c = I_a$ . peak ripple current voltage of capacitor is

Adv. A buck-boost regulator provides output voltage polarity reversal without transformer. It has high efficiency.



## Cuk - regulator :-

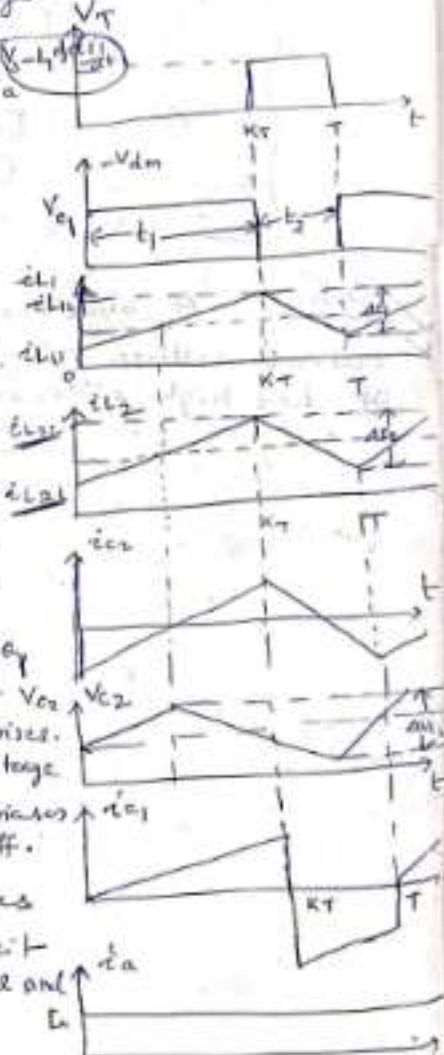
The Cuk regulator provides an output voltage which is less than or greater than the input voltage, but the output voltage polarity is opposite to that of input voltage.



Mode 1 : When transistor  $Q_1$  is turned on at  $t=0$ . The  $V_{ce}$  current through inductor  $L_1$  rises. At the same time, the voltage of capacitor  $C_1$  reverses biases diode  $D_m$  and turns it off.

The capacitor  $C_1$  discharges its energy to the circuit formed by  $C_1$ ,  $C_2$ , load and  $L_2$ .

Mode 2 When  $Q_1$  is turned off at  $t=t_1$ . The capacitor  $C_1$  is charged from input supply and the energy stored in the inductor  $L_1$  is transferred to the load. The diode  $D_m$  and  $Q_1$  provides synchronous switching action. The  $C_1$  is the medium for



transferring energy from the source and load.

The inductor  $L_1$  current rises linearly from  $I_{L11}$  to  $I_{L12}$  in time  $t_1$ .

$$V_s = L \frac{I_{L12} - I_{L11}}{t_1} = L_1 \frac{\Delta I_1}{t_1}$$

$$t_1 = \frac{\Delta I_1 L_1}{V_s}$$

Due to the charged capacitor  $C_1$ , the current of inductor  $L_1$  falls linearly from  $I_{L12}$  to  $I_{L11}$  in time  $t_2$ .

$$V_s - V_{C1} = -L_1 \frac{\Delta I_1}{t_2}$$

$$\Delta I_1 = \frac{V_s t_1}{L_1} = -\frac{(V_s - V_{C1}) t_2}{L_1}$$

$$t_1 = kT \quad t_2 = (-k)T$$

$$V_{C1} = \frac{V_s}{1-k}$$

The current of filter inductor  $L_2$  rises linearly from  $I_{L21}$  to  $I_{L22}$  in time

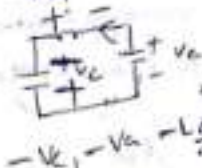
$$\frac{V_{C1} + V_a}{L_2} = \frac{I_{L22} - I_{L21}}{t_1} = L_2 \frac{\Delta I_2}{t_1}$$

$$t_1 = \frac{\Delta I_2 L_2}{\frac{V_{C1} + V_a}{L_2}}$$



$$V_a = -L_2 \frac{\Delta I_2}{t_2}$$

$$t_2 = -\frac{\Delta I_2 L_2}{\frac{V_a}{L_2}}$$



$$\Delta I_2 = \frac{(V_{C1} + V_a) t_1}{L_2} = -\frac{V_a t_2}{L_2}$$

Average voltage of capacitor  $C_1$  is

$$\frac{L_2 di}{dt} = V_{C1} + V_a$$

$$V_{C1} = \frac{V_a}{1-k}$$

$$V_{C1} = -\frac{V_a}{k}$$

$$V_a = -\frac{k V_{C1}}{1-k}$$

Assuming lossless  $V_s I_s = -v_a i_a = -V_s I_a k / (1-k)$

$$I_s = \frac{k I_a}{1-k}$$

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I_1 L_1}{V_s} - \frac{\Delta I_2 L_1}{V_s - V_{C1}} = \frac{-\Delta I_1 L_1 V_{C1}}{V_s (V_s - V_{C1})}$$

Peak to peak ripple current of inductor  $L_1$  is

$$\Delta I_1 = \frac{-V_s (V_s - V_{C1})}{f L_1 V_{C1}}$$

$$\Delta I_1 = \frac{V_s k}{f L_1}$$

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I_2 L_2}{V_{C1} + V_a} - \frac{\Delta I_2 L_2}{V_a}$$

$$= \frac{-\Delta I_2 L_2 V_{C1}}{V_a (V_{C1} + V_a)}$$

$$\Delta I_2 = \frac{-V_a (V_{C1} + V_a)}{f L_2 V_{C1}}$$

$$\Delta I_2 = \frac{-V_a (1-k)}{f L_2} = \frac{k V_s}{f L_2}$$

When transistor  $Q_1$  is off, the energy transfer capacitor  $C_1$  is charged by the input current for time  $t = t_2$ . The average charging current for  $C_1$  is  $I_{C1} = I_s$  and peak to peak ripple voltage of the capacitor  $C_1$  is

$$\Delta V_{C1} = \frac{1}{C_1} \int_0^{t_2} I_{C1} dt = \frac{1}{C_1} \int_0^{t_2} I_s dt$$

$$= \frac{I_s t_2}{C_1}$$

$$t_2 = \frac{v_s}{[(v_1 - v_c) f]}$$

$$\Delta v_{c1} = \frac{\epsilon_s v_s}{(v_c - v_a) f C_1}$$

$$\Delta v_{c1} = \frac{\epsilon_s (1-k)}{f C_1}$$

$$\Delta v_{c2} = \frac{1}{C_2} \int_0^{T/2} \epsilon_{c2} dt = \frac{1}{C_2} \int_0^{T/2} \frac{\Delta \epsilon_2}{4} dt = \frac{\Delta \epsilon_2}{8 f C_2}$$

$$\Delta v_{c2} = -\frac{v_a (1-k)}{8 C_2 L_2 f^2} - \frac{k v_s}{8 C_2 L_2 f^2}$$

$$t_2 = -\frac{\Delta \epsilon_2 L_2}{v_a}$$

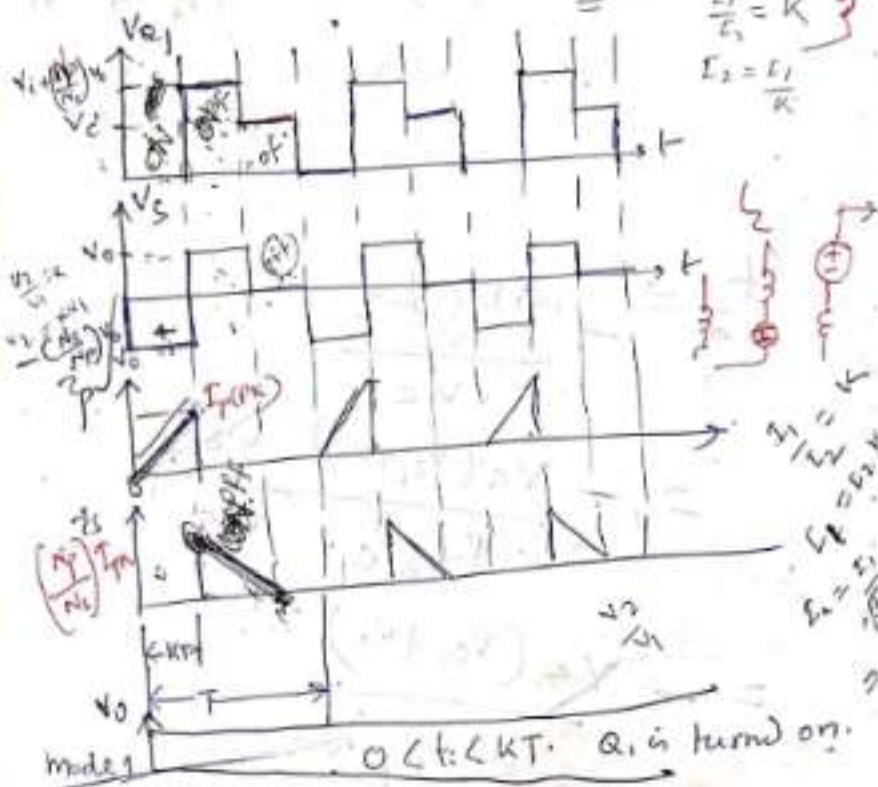
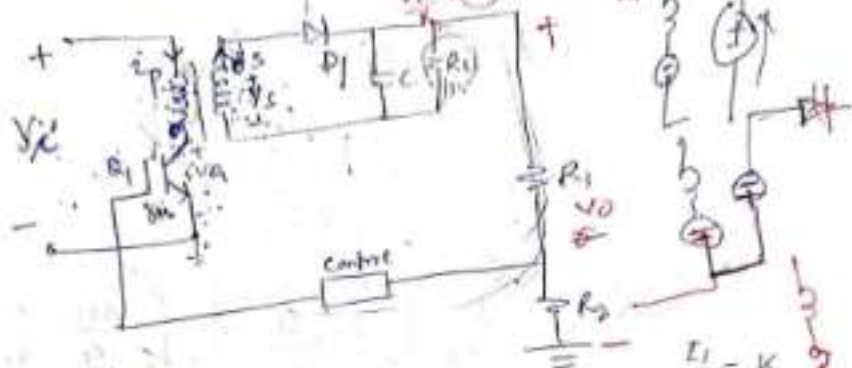
$$= -\frac{v_a (v_{c1} + v_s)}{f L_2 v_c}$$

$$= -\frac{v_a (v_{c1} + v_a)}{f v_c}$$

$$= -\frac{\left(-\frac{v_a}{k} + v_a\right)}{f} = \frac{\left(\frac{v_a}{k} - v_a\right) k}{-v_a f}$$

$$= \frac{v_a - k v_a}{-v_a f} = \frac{1-k}{-f}$$

# Flyback converter



$v = \frac{L di}{dt}$  The primary current  $i_p$  that increases linearly.

$$i_p = \frac{V_c t}{L_p}$$

$$i_p(\text{peak}) = \frac{V_s K T}{L_p}$$

The peak secondary current

$$I_1 = K \quad I_{sc(peak)} = \left( \frac{N_p}{N_s} \right) I_{p(peak)}$$

$\Rightarrow V_o = \frac{V_i}{K}$  This mode begins when switch  $Q_1$  mode 2 is turned off.

The secondary current that decreases linearly is given by

$$i_m = I_{sc(peak)} - \frac{V_o \cdot t}{L_s}$$

Because energy is transferred to the off during the time interval  $0$  to  $KT$ , the input power is given by

$$P_i = \frac{1}{2} L_p I_p^2(peak) = \frac{(K V_s)^2}{2 f L_p}$$

$$P_o = \eta P_i = \eta \frac{(V_o K)^2}{2 f L_p}$$

$$V_o = V_s K \sqrt{\frac{\eta R_L}{2 f L_p}}$$

$$K_{max} = \frac{V_o}{V_s(\min)} \sqrt{\frac{2 f L_p}{\eta R_L}}$$

$$V_o = V_s(\min) K_{max} \sqrt{\frac{\eta R_L}{2 f L_p}}$$

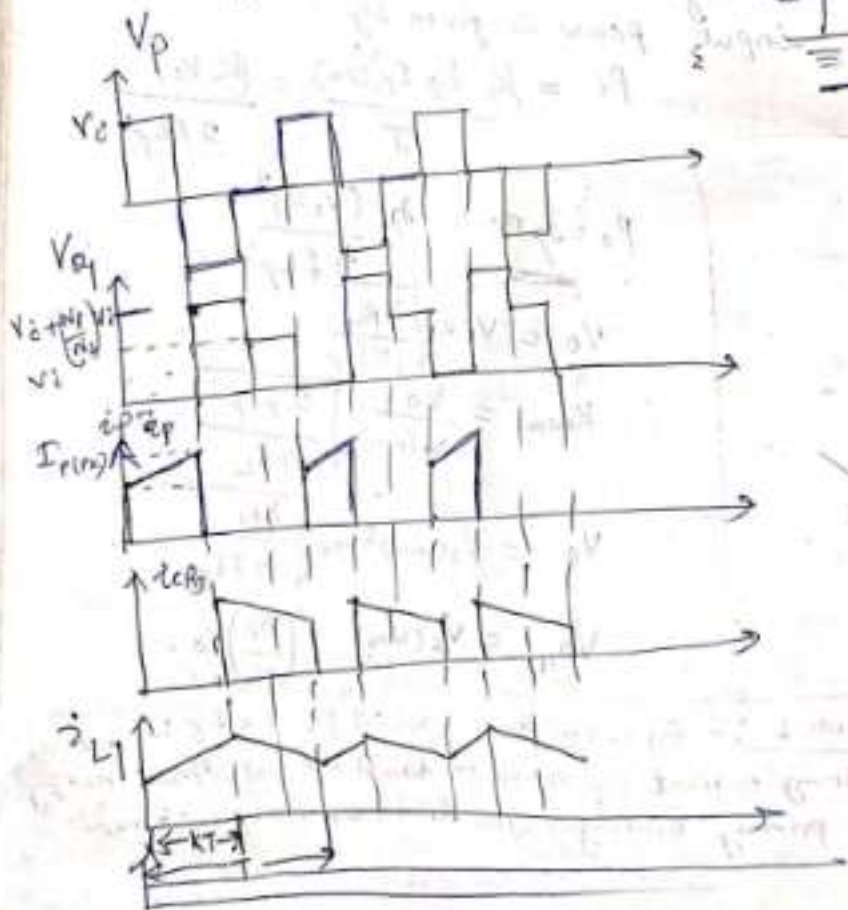
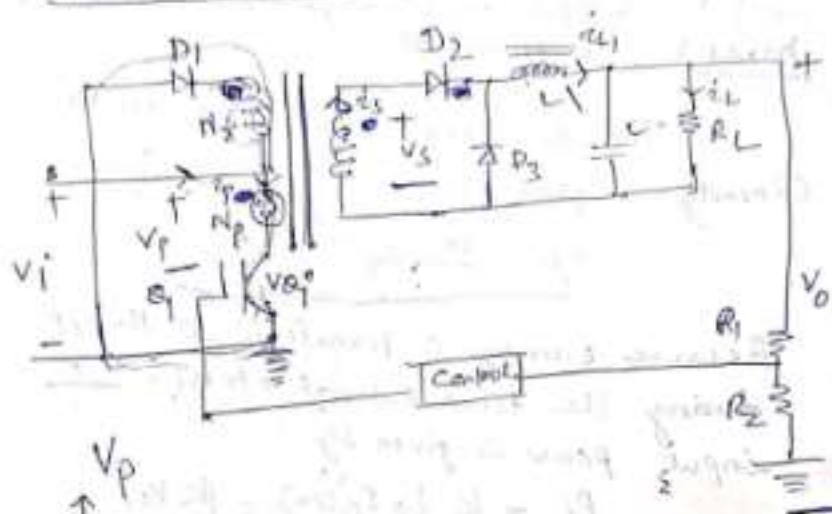
$$V_{o1} = V_s(\max) + \left( \frac{N_p}{N_s} \right) V_o$$

mode 1 :-  $Q_1$  is on and is valid for  $0 \leq t < KT$ . The primary current  $i_p$  starts to build up and store energy in primary winding. The diode  $D_1$  is reverse biased.

→ High output voltage at Low Power

→ Low Cost

### Forward Converter



→ Energy stored in the transformer core is returned to the supply and efficiency is increased.

→ The dot of the secondary winding of the transformer is so arranged that the o/p diode  $D_2$  is forward biased, when the voltage across the primary is positive.

Mode 1: — This mode begins when switch  $Q_1$  turns on. The voltage across the primary winding is  $V_s$ . The primary current  $i_p$  starts to build up and transfer energy from primary winding to the secondary and onto the  $L_p C$  filter and load  $R_L$  through the rectifier diode  $D_2$  which is forward biased.

$$i_p = \frac{N_s}{N_p} i_s$$

The magnetizing current  $i_{mag}$  that flows in the primary

$$i_{mag} = \frac{V_s}{L_p} t$$

$$i_p' = i_p + i_{mag} = \frac{N_s}{N_p} i_s + \frac{V_s}{L_p} t$$

$$I_{P(peak)} = I_{P(peak)} + \frac{V_s K T}{L_p}$$

$I_p(\text{pk})$  is the reflected peak current of the off inductor from the secondary  $I_p(\text{pk}) = \left(\frac{N_p}{N_s}\right) I_{L1}(\text{pk})$  ✓

$$\frac{I_1}{I_2} = \frac{N_2}{N_1}$$

$$I_1 \frac{N_p}{N_s} = I_2$$

$$V_{off} = \frac{N_s}{N_p} V_s \quad (\text{Voltage developed across the secondary winding})$$

$$\frac{di_{L1}}{dt} = \frac{V_s - V_o}{L_1}$$

$$I_{L1}(\text{pk}) = I_{L1}(0) + \frac{(V_s - V_o)}{L_1} \Delta t$$

Mode 2

This mode begins when  $G_1$  turns off. The polarity of the transformer voltage reverses. This causes  $D_2$  to turn off and  $D_1$  and  $D_3$  to turn on. While  $D_3$  is conducting energy is delivered to  $R_L$  through the inductor  $L_1$ . Diode  $D_1$  and the tertiary winding provide a path for the magnetizing current returning to the input. The current  $i_{L1}$  through the inductor  $L_1$ , which is equal to the current  $i_{D3}$  through diode  $D_3$  decreases linearly.

$$i_{L1} = i_{D3} = I_{L1}(\text{pk}) - \frac{V_o}{L_1} t$$

The off voltage  $V_o$  which is the time average of the secondary voltage, is given by

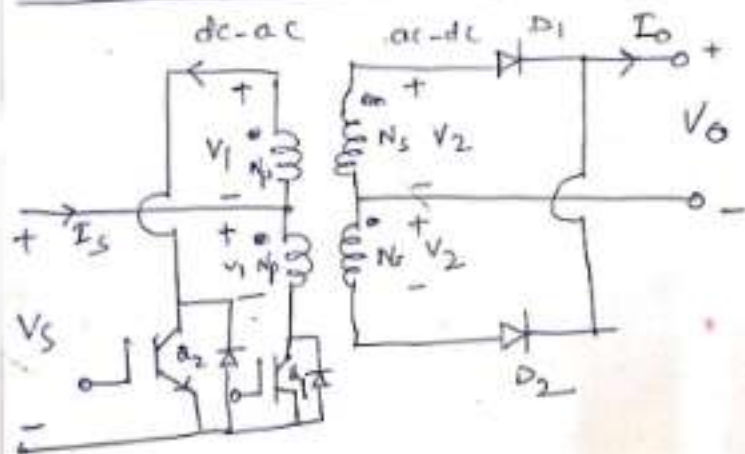
$$V_o = \frac{1}{T} \int_0^{kT} \frac{N_s}{N_p} V_s dt = \frac{N_s}{N_p} V_s k$$

$$I_c(\text{avg}) = I_p'(\text{avg}) = \left(\frac{N_p}{N_s}\right) I_{L1}(\text{pk}) + \frac{V_s k T}{L_1 D}$$

maximum collector voltage,  $V_{ce}$ , and of turn off  
 voltage is  $V_{Q_1(max)} = V_s(max) + V_r(max)$  with across  
 density only  
 $= V_s(max) \left(1 + \frac{N_1}{N_2}\right)$

$V_s K T = V_r (1 - K) T$  Adv: —  
 it is used with  
 power off below  
 200W.  
 Dis: —

### Push-pull Converter



- when  $Q_1$  is turned on,  $V_s$  appears across one-half of the primary
  - when  $Q_2$  is on,  $V_s$  is applied across the other half of the transformer. The voltage of a primary winding swings from  $-V_s$  to  $V_s$ .
  - The average current through the transformer should ideally be zero. The average output voltage is  $V_o = V_2 = \frac{N_s}{N_p} V_1 = a V_1 = a V_s$
- $Q_1$  and  $Q_2$  operates with 50% duty cycle.

The open ckt voltage is  $V_{oc} = 2V_s$   
 Average current of a transistor is  $I_{A1} = I_o/2$