DEPARTMENT OF ELECTRICAL ENGINEERING

GOVERNMENT COLLEGE OF ENGINEERING KALAHANDI

BHAWANIPATNA

Lecture Notes on Basic Electronics

By

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Field - Effect Transistors

The field-effect transistor (FET) is a three terminal device (namely drain, source and gate) used for a variety of applications.

Difference between the two types of transistors

BJT (Bipolar Junction Transistor)	FET (Field Effect Transistor)
i) BJT transistor is a current-controlled device.	i) FET is a voltage-controlled device.
ii) The current I_C is a direct function of the level of I_B.	ii) The current (O/P) is a function of the voltage V_{GS} applied to the input circuit.
iii) BJT is a bipolar device, the prefix bi reveals that the conduction level is a function of two charge carriers, electrons and holes	iii) The FET is a unipolar device depending solely on either electron or hole conduction.
iv) It has low input impendance.	iv) The FET is high input impendance.
v) BJT transistor has a much higher sensitivity to changes in the applied signal.	v) FET has lesser sensitivity to changes in the applied signal.
vi) BJTs are lesser temperature stable than FETs.	vi) FETs are more temperature stable than BJTs.
vii) BJTs are larger in construction than FETs.	vii) FETs are usually smaller in construction.

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There are two major categories of field-effect transistors

⟨i⟩ Metal-oxide semiconductor field-effect transistor (MOS-FET)

⟨ii⟩ Junction field-effect transistor (JFET)

METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS (MOSFET) :-

→ A MOSFET is a three terminal (source, gate and drain) device and drain current in it is controlled by the gate bias.

→ It is constructed with the gate terminal insulated from the channel, it is called insulated gate FET (IGFET).

→ MOSFET has lower capacitance and input impedance

MOSFETs are of two types

⟨i⟩ Enhancement type MOSFET (E-MOSFET)

⟨ii⟩ Depletion type MOSFET (DE-MOSFET)

Depletion-mode construction :-

A channel is physically constructed and a current between drain and source is due to voltage applied across the drain-source terminals.

Enhancement-mode construction :-

The enhancement MOSFET structure has no channel formed during its construction.

Depletion-Type MOSFET :-

N-channel depletion-type MOSFET :-

Basic construction :-

→ A slab of p-type material is formed from a silicon base and is referred to as the substrate.

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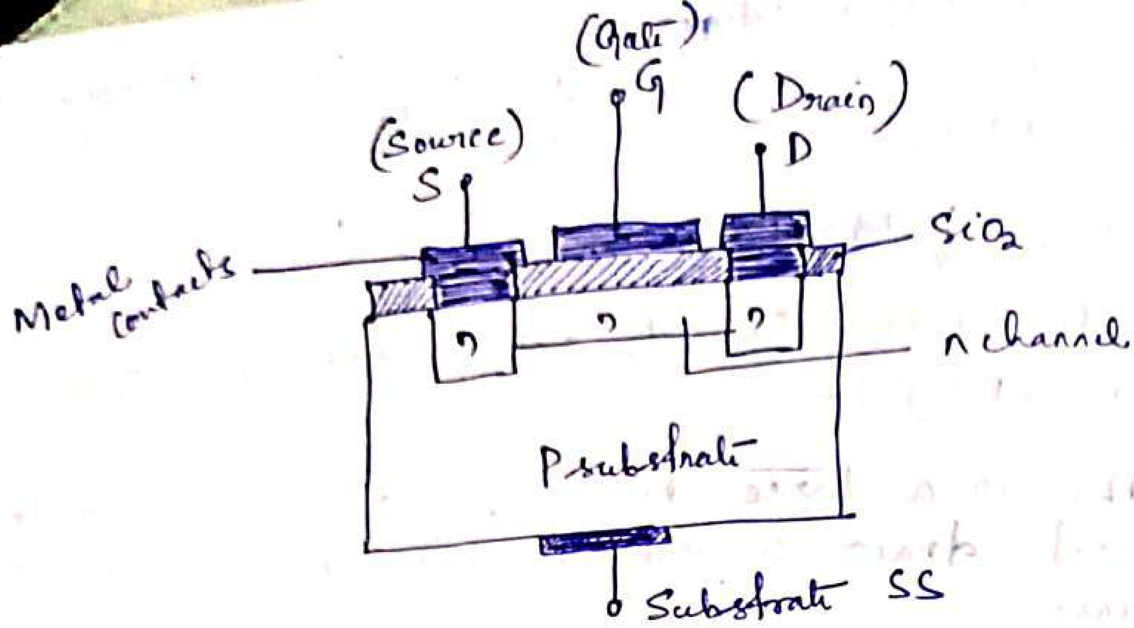


(n-channel depletion-type MOSFET)

→ It is the foundation upon which the device will be constructed.

→ In some cases the substrate is internally connected to the source terminal.

→ The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel.

→ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon ~~diode~~ dioxide (SiO_2) layer.

→ SiO_2 is a type of insulator referred to as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field.

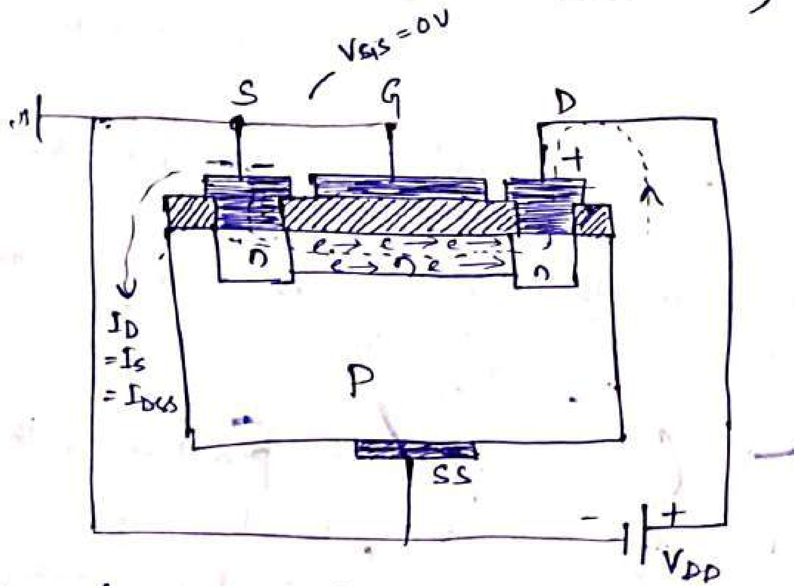
Functions of insulating layer :-

→ There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

→ It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very high input impedance of the device.

Basic operation and characteristics

Case-1 : $V_{GS} = 0V$ (Gate to source voltage is set to zero volts)



(n-channel depletion-type MOSFET with $V_{GS} = 0V$ and an applied voltage V_{DD})

→ $V_{GS} = 0V$ and V_{DS} is applied across the drain-to-source terminals.

→ The electrons are attracted towards the drain due to the positive terminal.

→ At $V_{GS} = 0V$, the current is $I_D = I_{DSS}$.

I_{DSS} = Drain-source saturation current

Case-2 : ($V_{GS} = -1V$) (V_{GS} is set at a negative voltage as $-1V$)

→ The negative potential at the gate will tend to pressure electrons towards the p-type substrate and attract holes from the p type substrate.

→ Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction.

→ The more negative the bias, the higher is the rate of recombination.

→ The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.

<u>Case-3</u> (V_{GS} = +ve V) (V_{GS} is set at positive voltage)

→ For positive values of V_{GS}, the positive gate draws additional electrons from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between the accelerating particles.

→ As the gate-to-source voltage continues to increase in the positive direction, the drain current will increase at a rapid rate.

→ Thus, the application of a positive gate-to-source voltage has "<u>enhanced</u>" the level of free carriers in the channel compared to that encountered with V_{GS} = 0V.

→ For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the <u>enhancement region</u> with the region between cutoff and the saturation level of I_{DSS} referred to as the <u>depletion</u> region.

— The relationship between I_D and V_{GS} is defined by <u>Shockley's equation</u>

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

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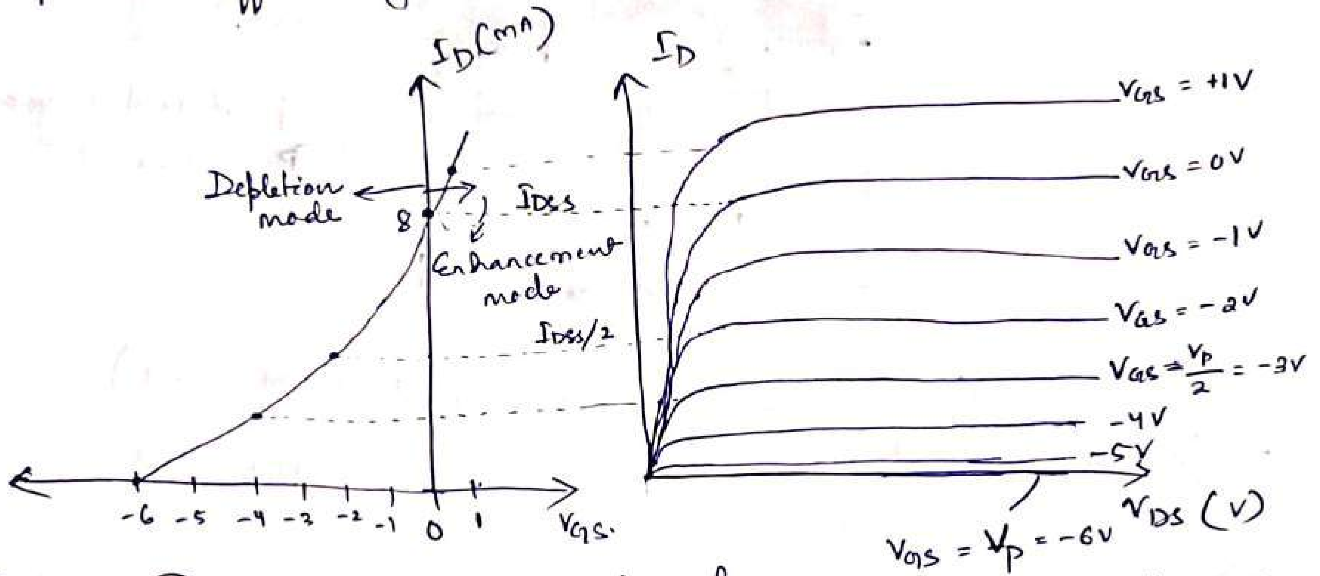
I_D = Drain current

I_{DSS} = Drain-source saturation current

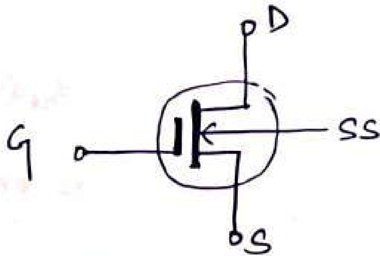
V_{GS} = Gate-to-source voltage

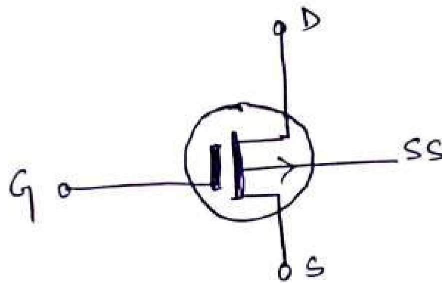
V_P = pinch-off voltage

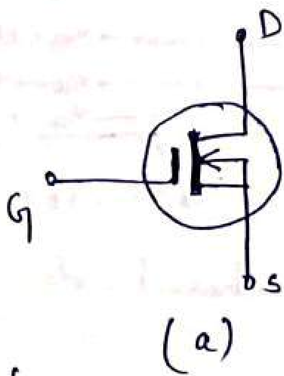


(Drain and transfer characteristics for an n-channel depletion-type MOSFET)

Graphic Symbols

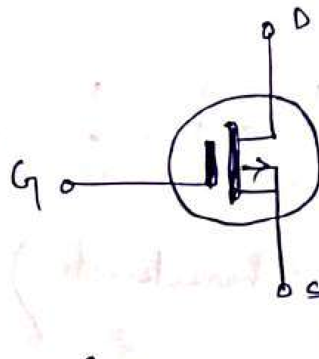






(a)

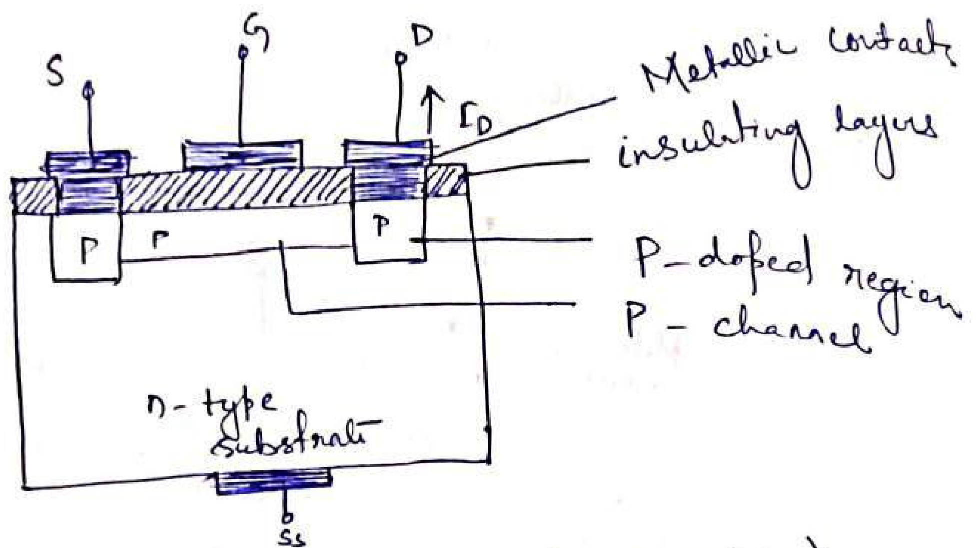
(n-channel depletion-type MOSFET)



(b)

(P-channel depletion-type MOSFET)

P-channel Depletion-Type MOSFET

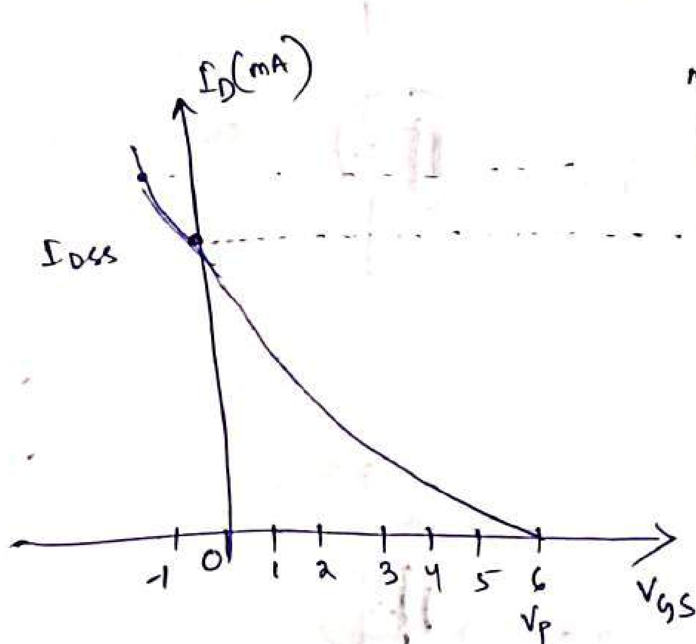


(P-channel depletion-type MOSFET)

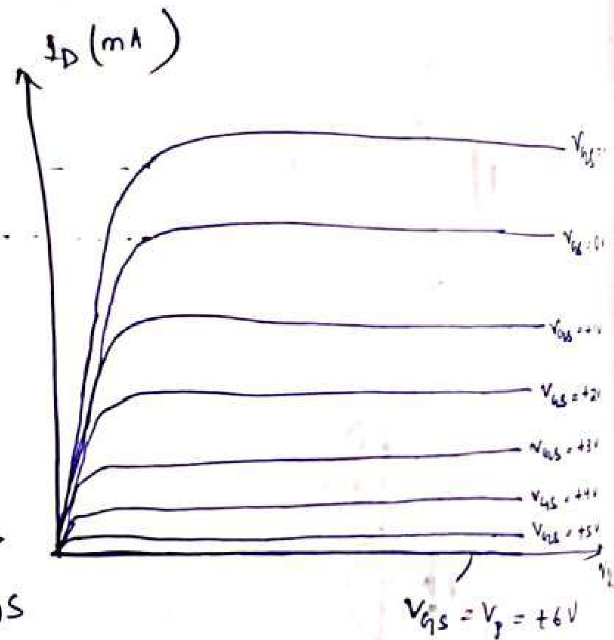
→ The construction of a p-channel depletion-type MOSFET is reverse of that of n-channel MOSFET.

→ There is n-type substrate and p-type channel.

→ The drain current increases from cutoff at $V_{GS} = V_p$ in the positive V_{GS} region to I_{DSS} and continues to increase for increasingly negative value of V_{GS}.



(Transfer characteristic)

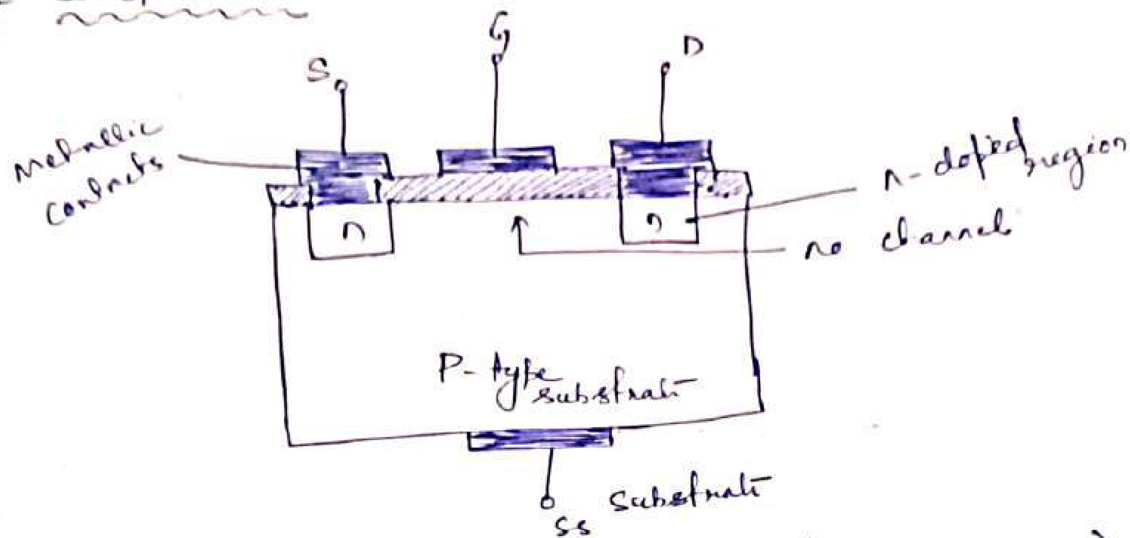


(Drain characteristic)

Enhancement - Type MOSFET

n-channel enhancement - type MOSFET :-

Basic Construction



(n-channel enhancement-type MOSFET)

→ A slab of p-type material is formed from a silicon base and is referred to as the substrate.

→ The substrate is sometimes internally connected to the source terminal.

→ The source and drain terminals are connected through the metallic contacts to n-doped regions.

→ There is absence of channels between the two n-doped regions.

→ The SiO_2 layer is present to isolate the gate metallic platform from the region between the drain and source.

Basic operation and characteristics.

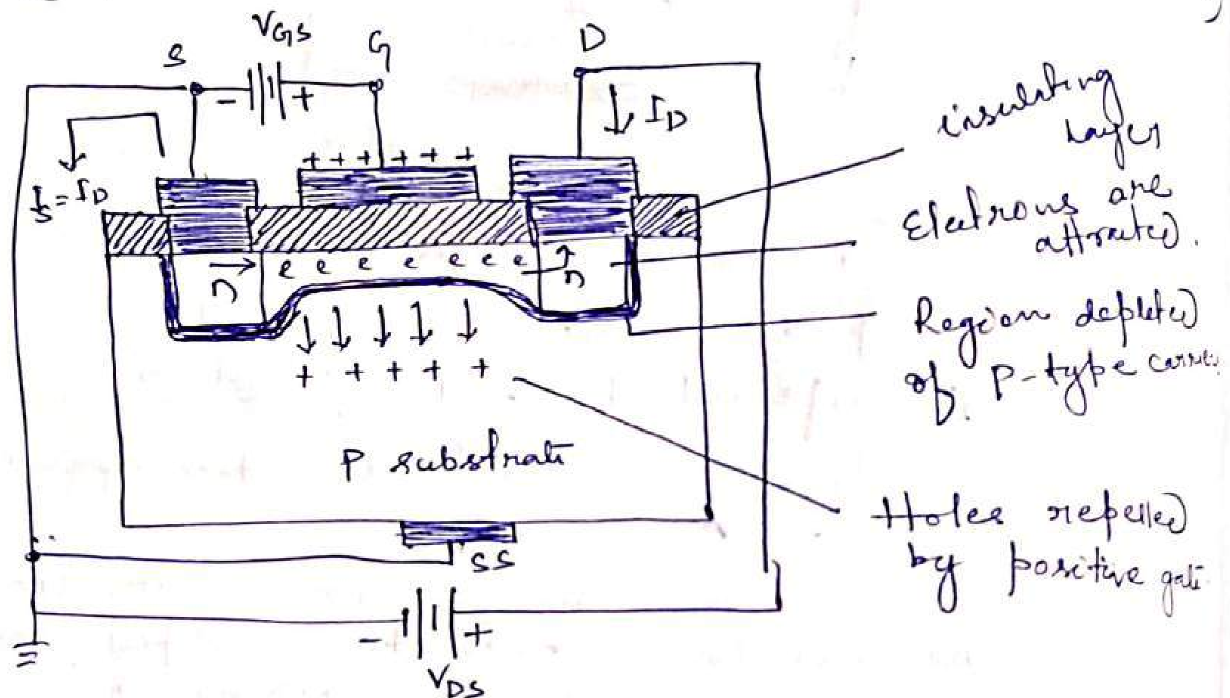
Case - 1 ($V_{GS} = 0V$) (V_{GS} is set at 0V)

→ If V_{GS} is set at 0V and a voltage applied between drain and the source of the device results in a current of effectively '0A' due to the absence of an n-channel.

→ It is not sufficient to have large accumulation of carriers at the drain and the source if a path fails to exist between the two.

→ With V_{DS} some positive voltage, V_{GS} at 0V and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

Case-2 (V_{GS} = +ve , $V_{GS} > V_T$; V_T = threshold voltage)



(Channel formation in the n-channel enhancement-type MOSFET)

→ Both V_{DS} and V_{GS} have been set at positive voltage greater than 0V establish the drain and the gate at a positive potential with respect to source.

→ The positive potential at the gate repels the holes in the p-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate.

→ The electrons in the p-substrate (minority carriers of the material) are attracted to the positive gate

and are accumulated in the region near the surface of the SiO_2 layer.

→ The SiO_2 layer and its insulating qualities prevent the negative carriers from being absorbed at the Gate terminal.

→ As V_{GS} increases in magnitude the concentration of electrons near the SiO_2 surface increases which induces the flow of current between drain and source.

→ The level of V_{GS} that results in the significant increase in drain current is called the <u>threshold voltage</u> and is given by V_T.

→ Since the channel is absent at $V_{GS} = 0V$ and enhanced by the application of positive V_{GS}, this type of MOSFET is called an <u>enhancement type</u> MOSFET.

<u>Case - 3</u> ($V_{GS} > 0V$, $V_{GS} > V_T$ (but constant), V_{DS} increases)

→ If V_{GS} is constant, V_{DS} increases, Gate-to-drain voltage decreases as per equation

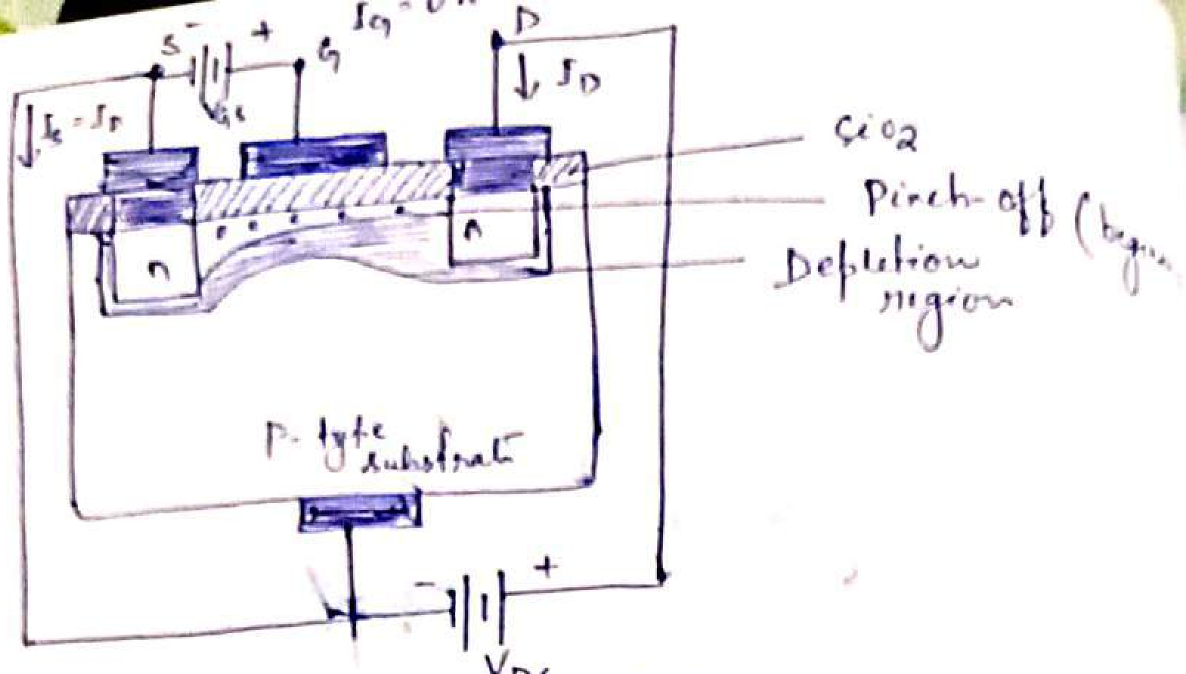
$$V_{DG} = V_{DS} - V_{GS}$$

→ This reduces the attractive forces for free electrons in this region of the induced channel, causing a reduction in the effective channel width.

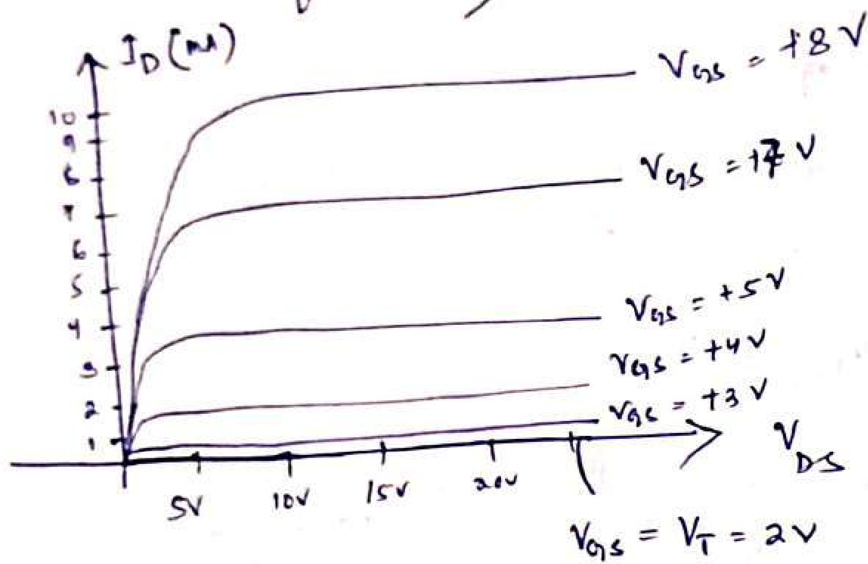
→ Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established.

→ Any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown condition is achieved.

$$V_{DSsat} = V_{GS} - V_T$$



(Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS})



$V_{GS} = V_T = 2V$

(Drain characteristics of an n-channel enhancement type MOSFET)

→ For values of V_{GS} less than the threshold level, the drain current of an enhancement type MOSFET is 0mA.

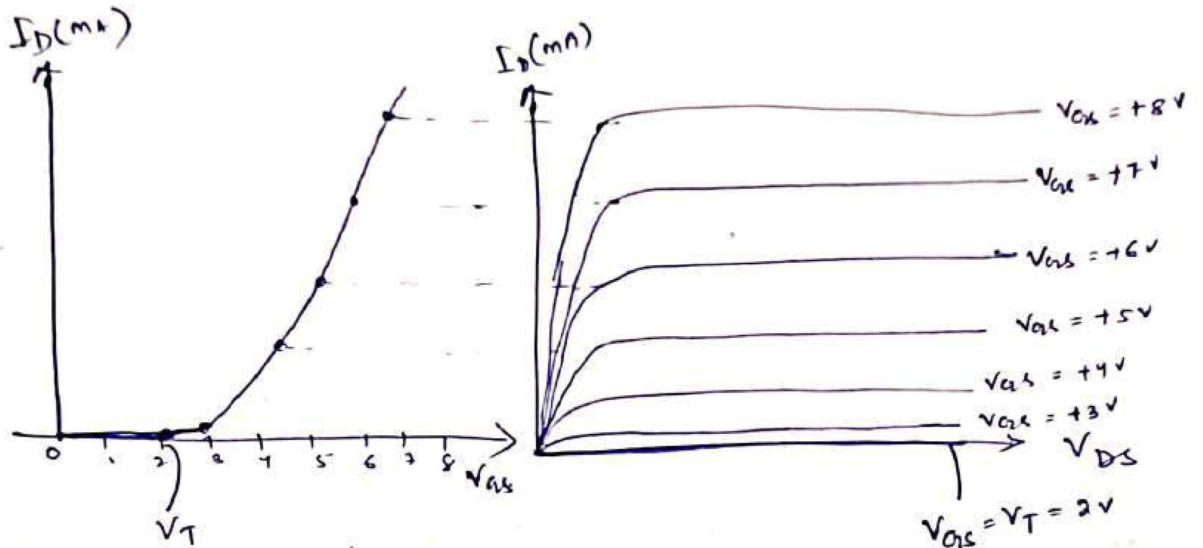
→ For $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following relationship as

$$I_D = K\left(V_{GS} - V_T\right)^2$$

K = constant and is a function of the construction of the device.

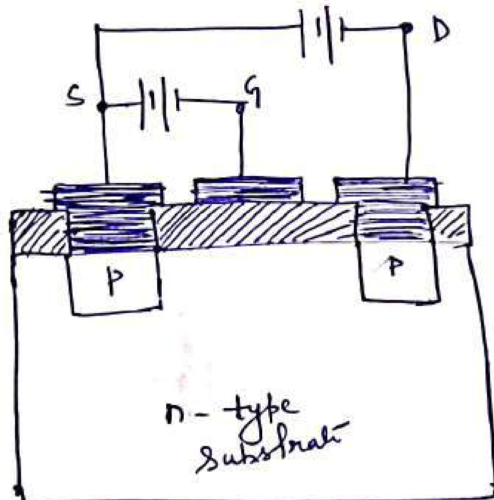
$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

Transfer characteristics



(Transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics)

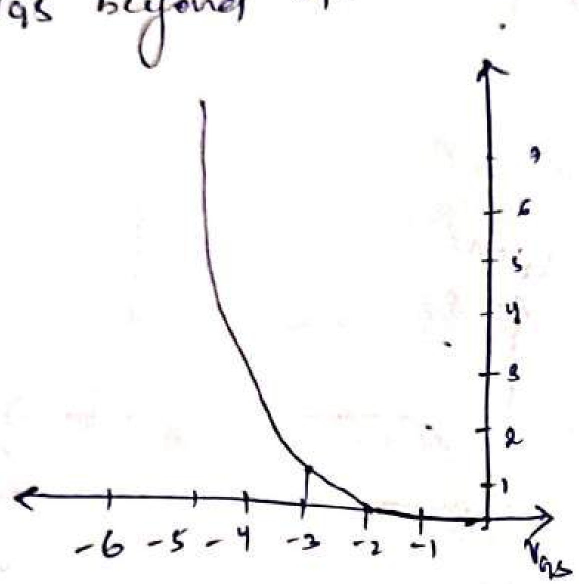
P channel Enhancement type MOSFET :



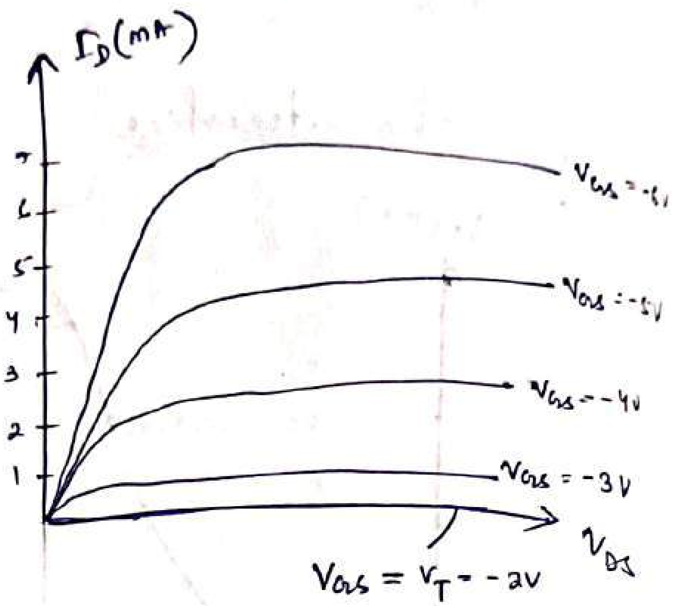
(P-channel enhancement-type MOSFET)

→ Here, an n-type substrate and p-doped regions are taken under the drain and source connections.

→ I_D increases with increasing negative values of V_{GS} beyond V_T.

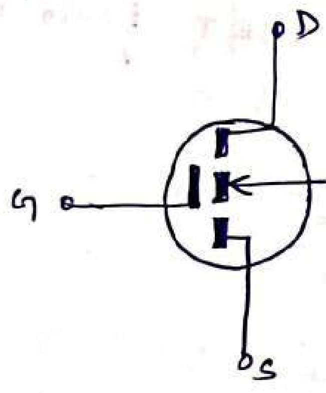


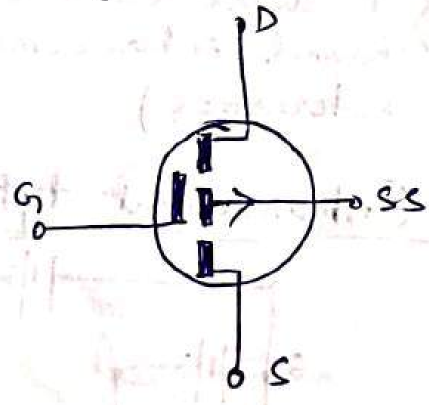
(Transfer characteristic)

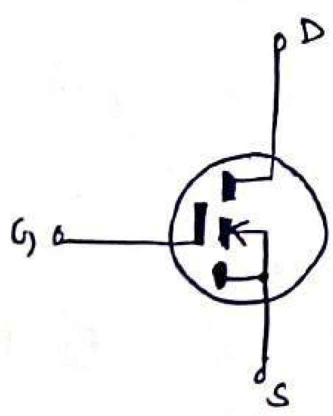


(Drain characteristic)

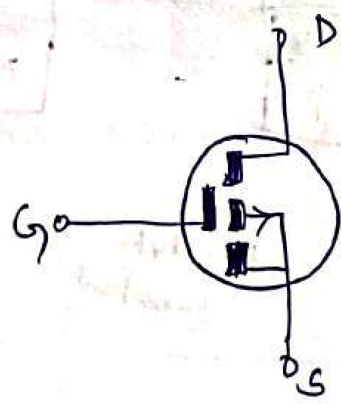
Symbols for enhancement-type MOSFETs







(n-channel enhancement type MOSFET)



(p-channel enhancement type MOSFET)

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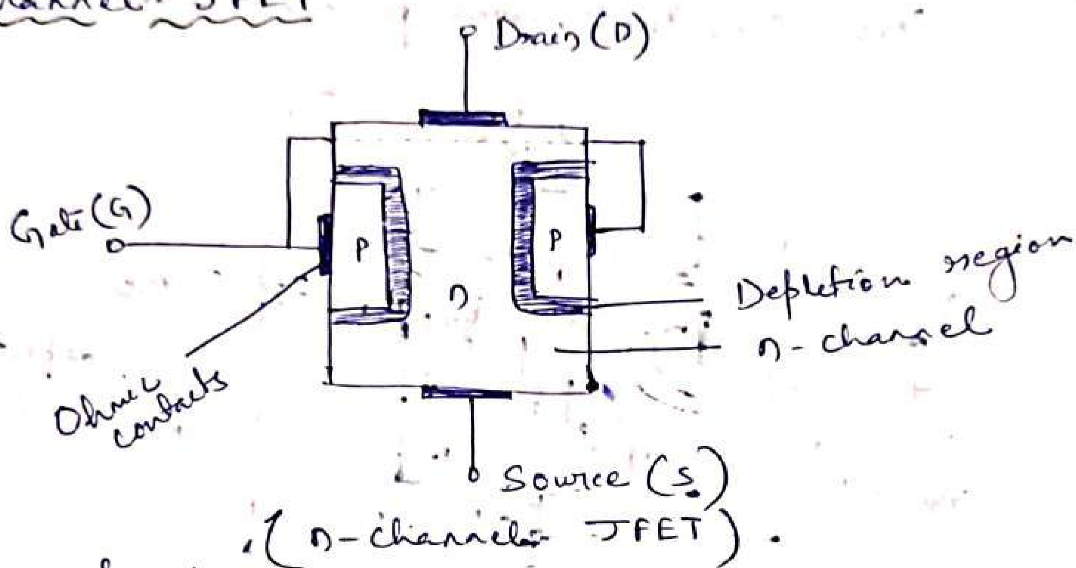
Junction Field Effect Transistors (JFET)

JFETs are two types
⟨i⟩ n-channel JFET
⟨ii⟩ P-channel JFET

n-channel JFET



(n-channel JFET).

Basic construction :-

→ In the n-channel JFET an n-type Silicon bar is referred to as the channel, has two smaller pieces of p-type Si material diffused on the opposite sides of its middle part, forming P-N Junction.

Source (S) :- The terminal through which the majority carriers enter the channel is called the Source terminal (S).
The conventional current entering the channel at S is represented as I_S.

Drain (D): The terminal through which the majority carriers leave the channel is called the drain terminal (D).
The conventional current leaving the channel at D is denoted as I_D.

Gate (G): The two P-n junctions forming diodes or gates are connected internally in a common terminal, is called the Gate terminal. The gate controls the potential to the drain.

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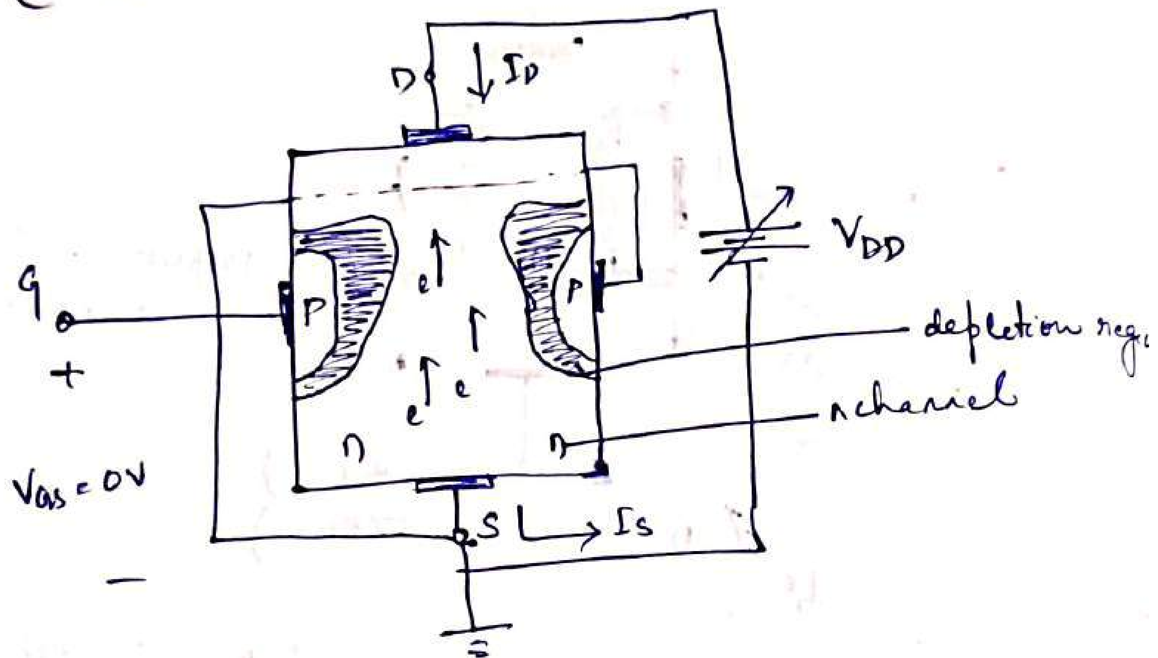
Working Principle

The potential across Gate and Source is denoted as V_{GS}.

The potential across Drain and Source is denoted as V_{DS}.

Case - I ($V_{GS} = 0V$, V_{DS} = some positive value)



($JFET$ at $V_{GS} = 0V$ and $V_{DS} > 0V$)

→ A positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0V$.

→ The gate and source terminal at the same potential and a depletion region in the low end of each p-material similar to the distribution of the no-bias condition.

→ When V_{DS} is applied, the electrons are drawn to the drain terminal.

It is observed that

$$I_D = I_S$$

I_D = Drain current

I_S = Source current

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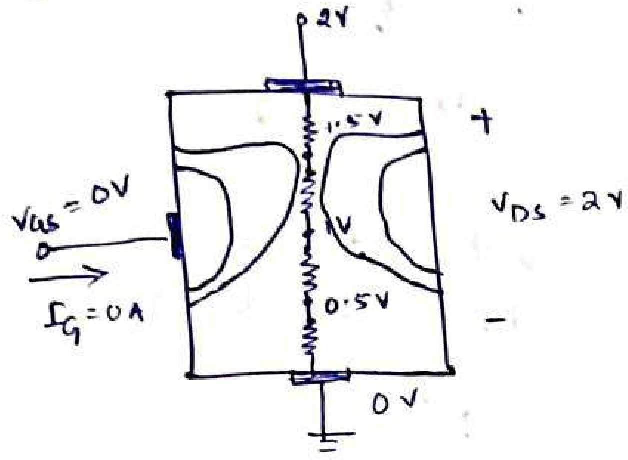
→ The flow of charge is limited by the resistance of the n-channel between drain and source.

→ It is important to note that the depletion region is wider near the top of both p-type materials.

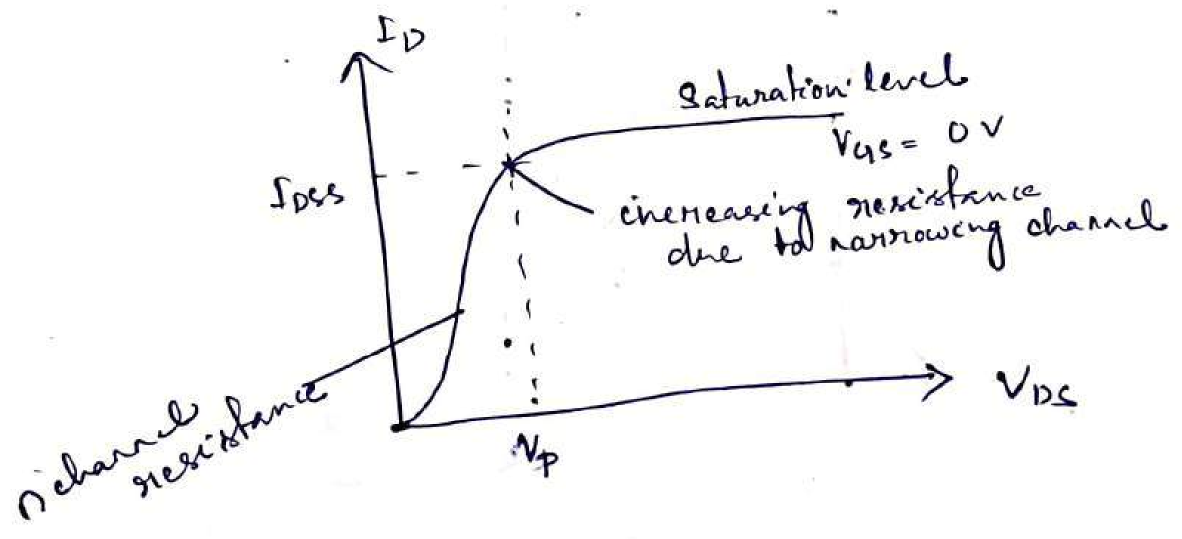


(Varying reverse-bias potentials across the p-n junction of an n-channel JFET)

→ Assuming a uniform resistance in the n-channel, the resistance of the channel is broken down into divisions.

→ The upper region is reverse-biased by 1.5V and lower region is reverse-biased by 0.5V.

→ The p-n junction is reverse-biased for the length of the channel results in a gate current of zero amp.



(I_D versus V_{DS} for $V_{GS} = 0V$)

→ As V_{DS} is increased from 0V to a few volts, the current will increase by Ohm's law.

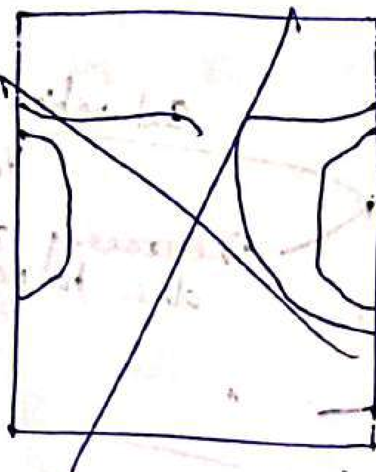
→ The plot reveals that the resistance is essentially constant for the region of low values of V_{DS}.

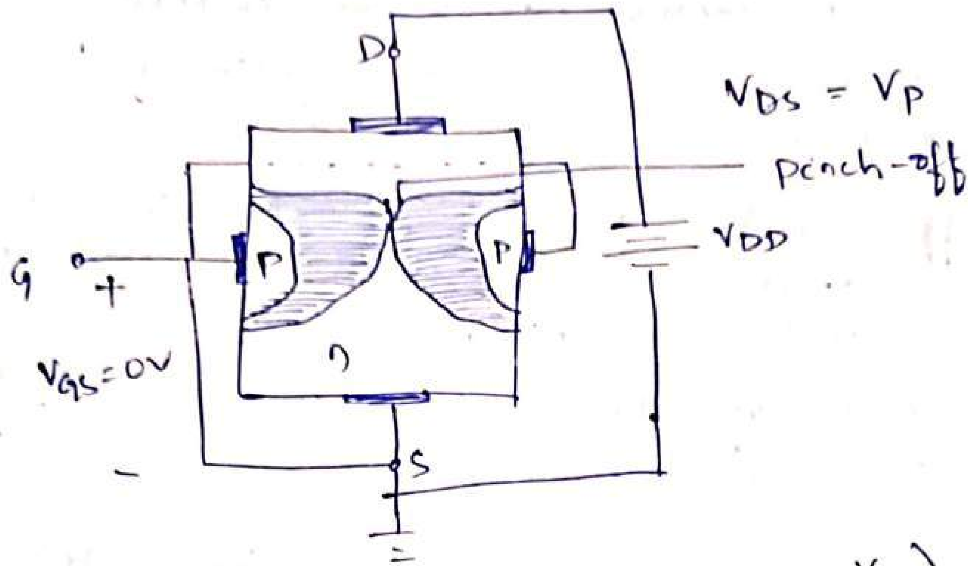
→ As V_{DS} increases and approaches a level referred to as V_P, the resistance increases.

→ If V_{DS} is increased to a level, it appears that two depletion regions would touch resulting in a condition referred to as <u>pinch-off</u>.

→ The level of V_{DS} that establishes this condition is referred to as the <u>pinch-off voltage</u> and is denoted by V_P.

At this voltage I_D maintains a saturation level defined as <u>I_{DSS}</u>.





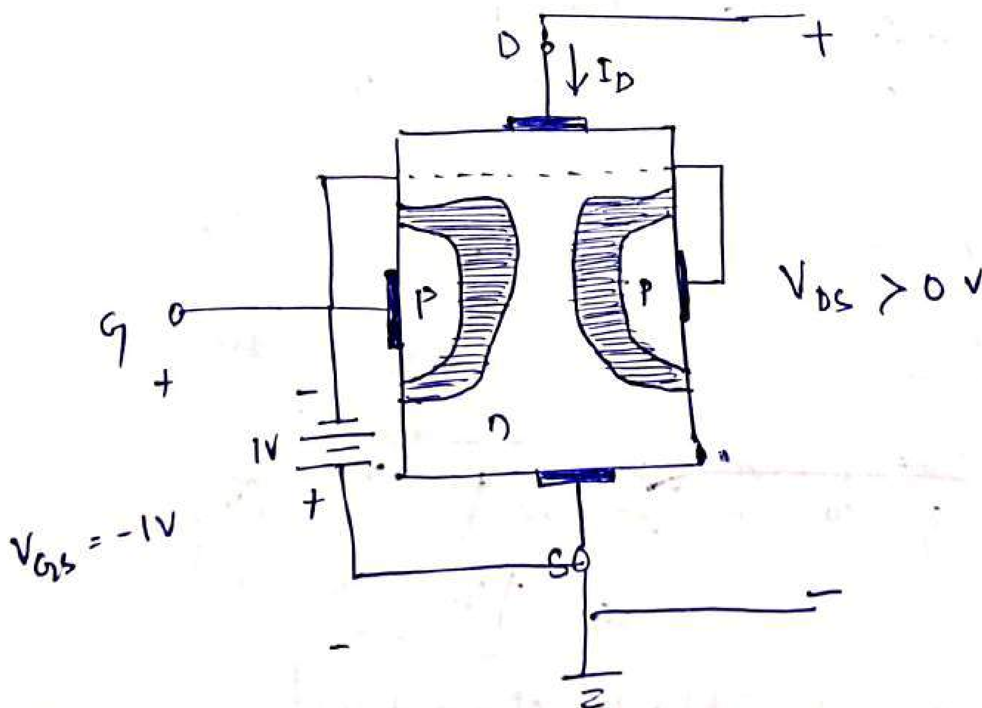
(Pinch-off , $V_{GS} = 0V$, $V_{DS} = V_P$)

I_{DSS} = drain to source current with a short-circuit connection from gate to source / Drain to source saturation current

<u>I_{DSS}</u> is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0V$ and $V_{DS} > |V_P|$

<u>Case - II</u> ($V_{GS} < 0V$)

- The voltage from gate to source is denoted as <u>V_{GS}</u> which is the <u>controlling voltage</u> of the JFET.



(Application of negative voltage to the gate of a JFET)

→ For the n-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0V$ level.

→ The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0V$, but at lower levels of V_{DS}.

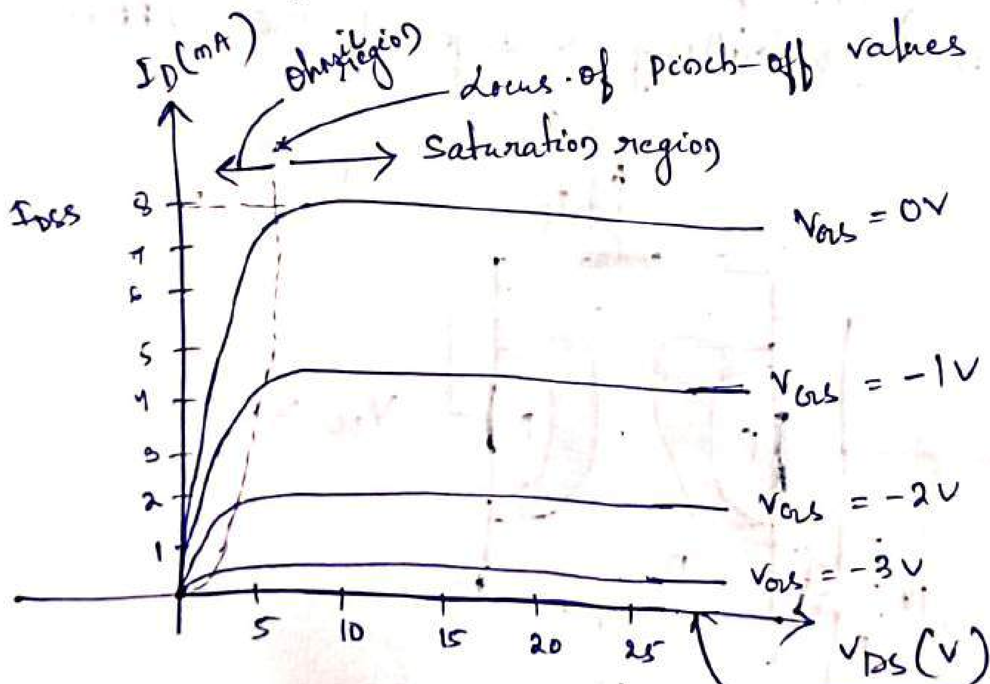
→ The result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}.

→ Eventually, V_{GS} when $V_{GS} = -V_p$ will be sufficiently negative to establish a saturation level that is 0mA. The device is turned off.

★ Imp The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_p$ with V_p is -ve.

V_p = -ve for n-channel devices

V_p = +ve for p-channel devices.



(n-channel JFET characteristics)

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Voltage - Controlled Resistor

Locus of pinch-off values :- The line joining the pinch-off voltage of each characteristic curve.

→ The region to the left of the pinch-off locus is referred to as the ohmic/ voltage controlled resistance region.

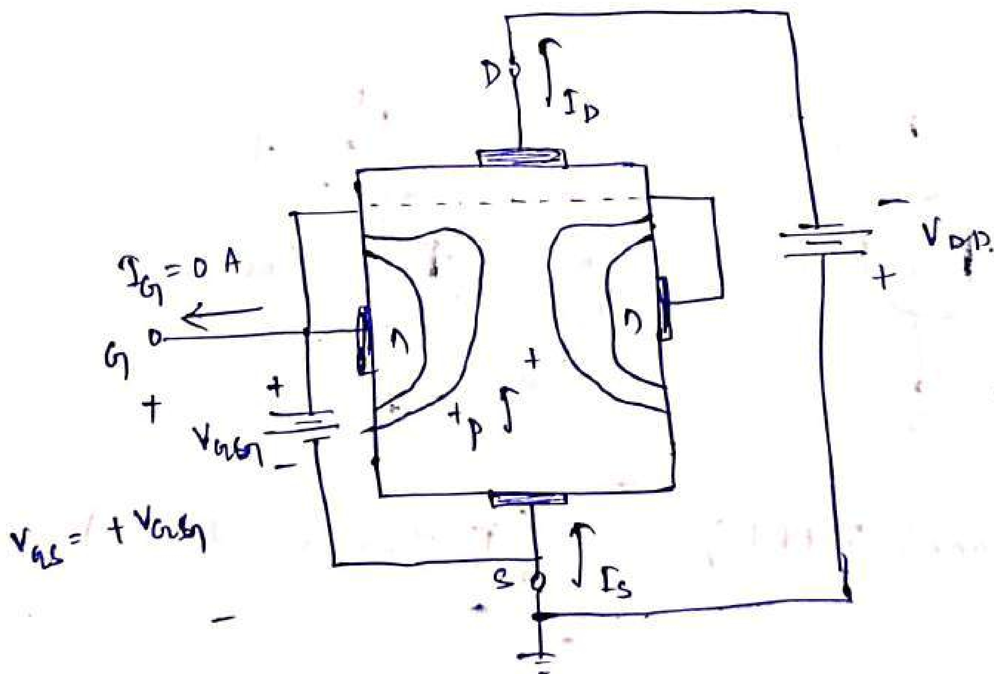
In this region an JFET can be employed as a variable resistor where resistance is controlled by V_{GS}.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

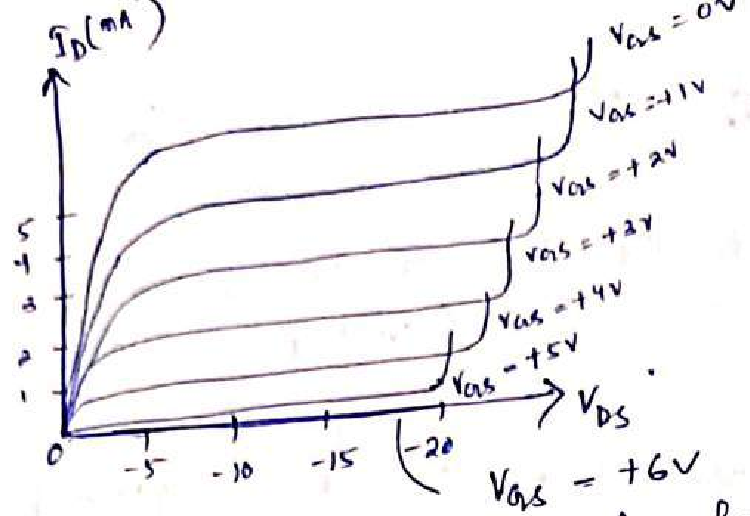
r_o = resistance with $V_{GS} = 0\,V$

r_d = resistance of the JFET at the given value of V_{GS}.

P- channel Devices



(P-channel JFET)



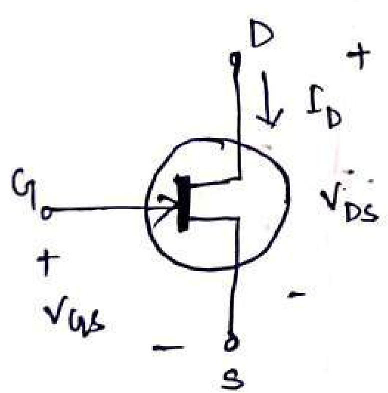
(P-channel JFET characteristic)

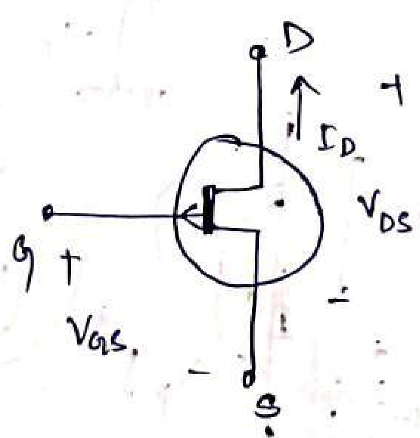
→ The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}.

→ For the p-channel device the channel will be constricted by increasing positive voltages from gate to source.

→ At high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred.

Symbols





(n-channel JFET)   (P-channel JFET)

Transfer characteristics

- The relationship between I_D and V_{GS} is defined by Schockley's equation:

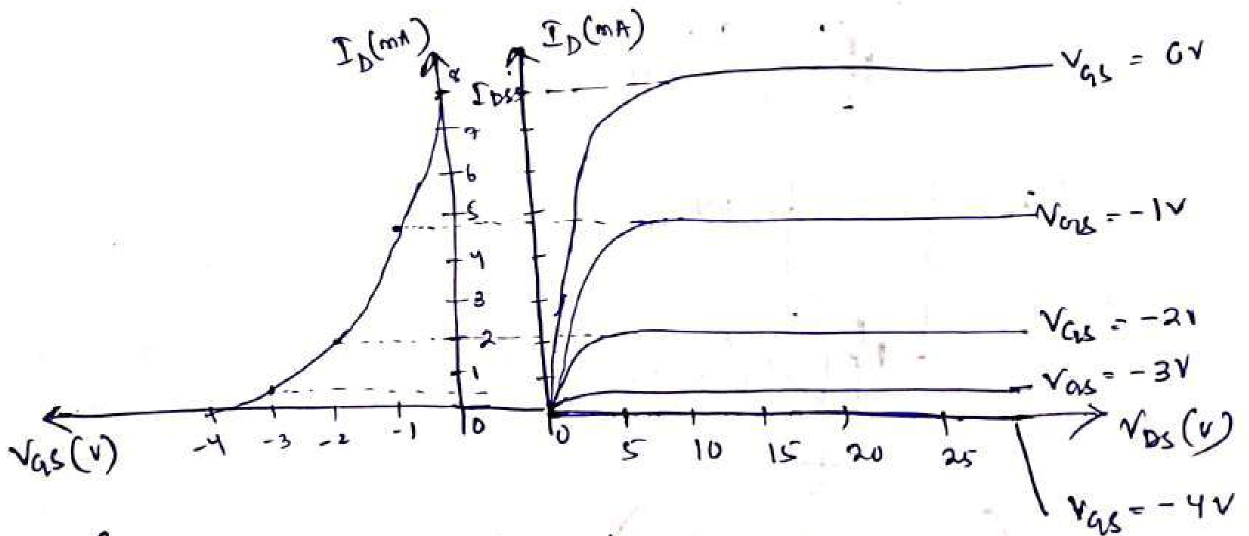
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

I_{DSS}, V_P = constants
V_{GS} = Control variable

- The squared term results the nonlinear relationship between I_D and V_{GS}.

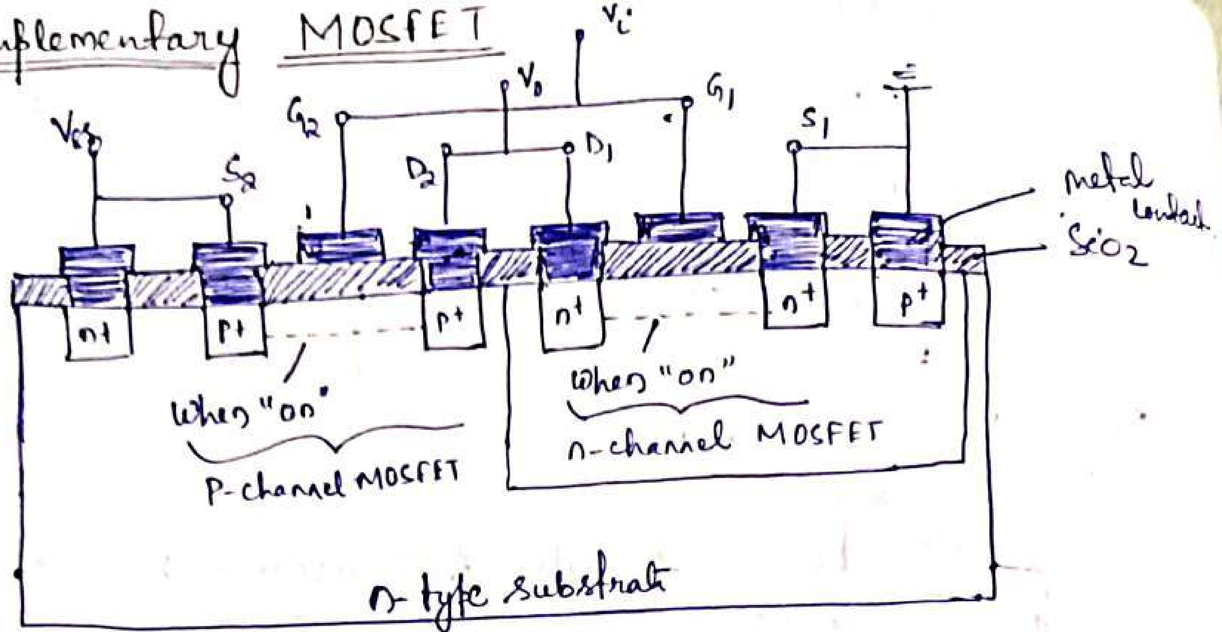
→ The <u>transfer</u> <u>characteristics</u> are a plot of an output (or drain) current versus an input-controlling quantity (V_{GS}).

→ The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.



(Obtaining the transfer curve from the drain characteristics)

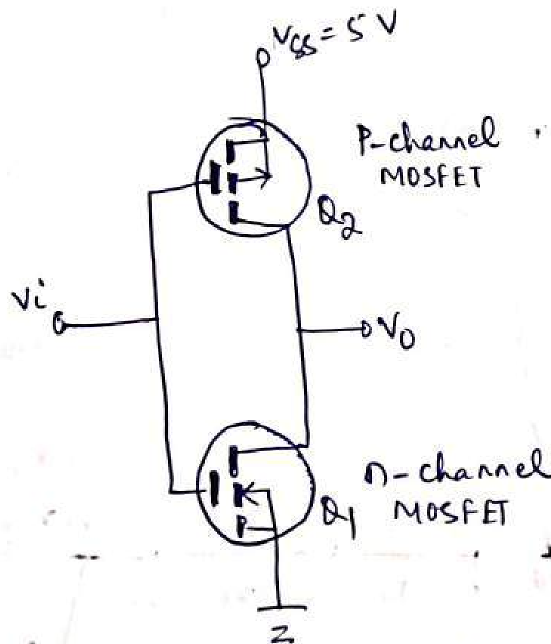
Complementary MOSFET



(CMOS with connections)

→ A very effective logic circuit can be established by constructing a p-channel and n-channel MOSFET on the same substrate.

→ Effective application of CMOS is an inverter.



(CMOS inverter)

→ An inverter is a logic circuit that inverts the applied signal.

→ As shown in the figure, gates of both p-channel and n-channel MOSFET are commonly connected to the applied signal V_i.

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→ Drains of both MOSFETs are connected to V_0.
→ The source of the p-channel MOSFET is connected directly to the applied voltage V_{SS} and the source of the n-channel MOSFET (Q_1) is connected to ground.

As we know

n-channel enhancement MOSFET is ON ⇒ $V_{GS} \geq V_T$
p-channel enhancement MOSFET is ON ⇒ $V_{GS} \leq V_T$

when $V_i = 5V$, Q_1 is ON and Q_2 is OFF.
Hence Q_1 offers a very low resistance path and Q_2 induces a high resistance path or in OFF condition.

$$V_{out} = 0V \text{ (called 0 state)}$$

Similarly when $V_i = 0V$, Q_1 is OFF and Q_2 is ON.

$$V_{out} = V_{SS} = 5V \text{ (called 1 state)}$$

→ It is used in computer logic design.

input	logic state	Transistor status Q_1	Transistor status Q_2	Output $V_0(V)$	logic state
5	1	ON	OFF	0	0
0	0	OFF	ON	5	1

→ Since the drain current that flows for either case is limited by the OFF transistor to the leakage value, the power dissipated by the device in either state is very low.

Characteristics

→ High input impedance
→ fast switching speeds
→ Lower operating power levels

Integrated Circuits

Integrated circuit :-

An integrated circuit is one in which various components such as resistors, capacitors, diodes and transistors are fabricated on a small semiconductor chip.

→ An integrated circuit consists of a number of circuit components (Eg. transistors, diodes, resistors etc.) and their inter connections in a single small package to perform complete electronic function.

→ The size of an IC is extremely small. It shows a typical semiconductor chip having dimensions 0.2 mm × 0.2mm × 0.001 mm.

Advantages

(i) Increased reliability due to lesser number of connections

(ii) Extremely small size due to fabrication of various circuit elements

(iii) Lesser weight and space requirement

(iv) Low power requirements

(v) Low cost.

(vi) The circuit lay out is greatly simplified.

IC Package & Classifications

→ The IC units are fast replacing the discrete components in all electronic equipment.

Four Basic types of constructions are employed in the manufactures

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(i) Mono-lithic (iii). Thick-film

(ii) Thin-film (iv) Hybrid

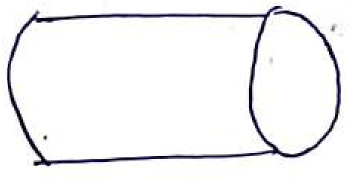
Monolithic IC

A monolithic IC is one in which all circuit components and their interconnects are formed on a single thin wafer called the substrate.

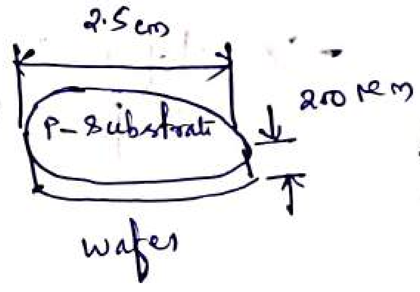
The basic production processes for the monolithic IC are as follows..

(i) P-Substrate :-

A cylindrical P-type si crystal is grown having typical dimensions 25 cm long and 2.5 cm diag diameter. The typical thickness of the wafer is 200 Rem. The ICs are produced on this wafer.



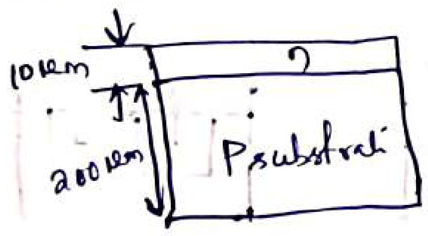
P-type si crystal

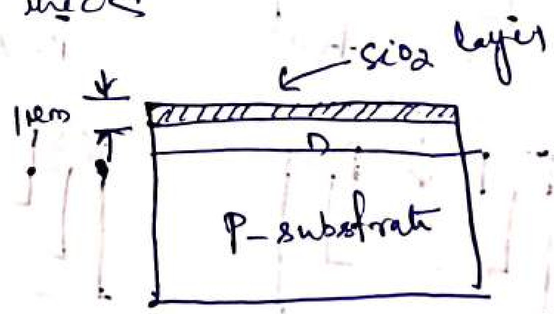


wafer

(ii) Epitaxial n layer :-

A gax mixture of si atoms and pentavalent atoms is passed over the wafers. This forms a thin layer of n-type semiconductor on the heated surface of substrate. This thin layer is called the epitaxial layer and is about 10 Rem thick.



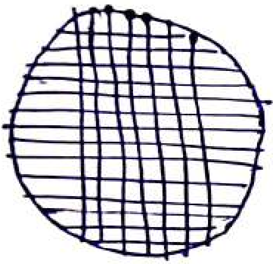


(iii) **Insulating layer :-** In order to prevent the contamination of the epitaxial layer, a thin SiO_2 layer about 1 μm thick is deposited over the entire surface.

(iv) **Producing Components :-**
By the process of diffusion, appropriate materials are added to the substrate at specific locations to produce diodes, transistors, resistors and capacitors.

(v) **Etching :-**
Before any impurity is added to the substrate, the exposed oxide layer is etched. The process of etching exposes the epitaxial layer and permits the production of desired components.

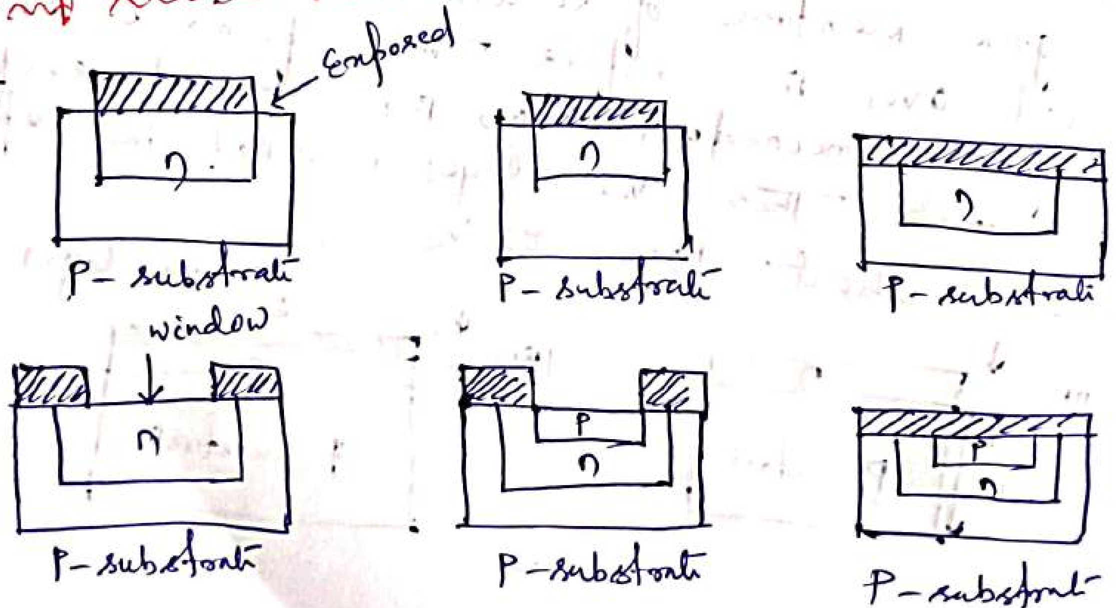
(vi) **Chips :-**



→ Wafer is divided into small chips by a process similar to glass cutting.

Integration of circuit Components :-

(i) **Diodes :-**



→ Part of SiO_2 layer is etched off, exposing the epitaxial layer.

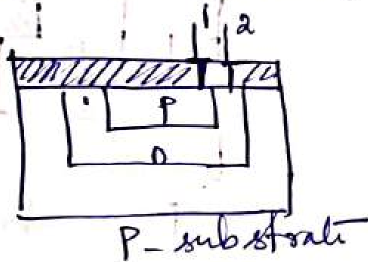
→ The wafer is then put into a furnace and trivalent atoms are diffused into the epitaxial layer. Thus we get an island of n-type material under the SiO_2 layer.

→ Next pure oxygen is passed over the wafer to form a complete SiO_2 layer.

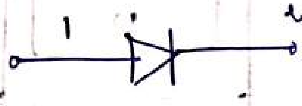
→ A hole is then etched at the centre of this layer; thus exposing the n- epitaxial layer.

→ The hole in SiO_2 layer is called a window. The trivalent atoms diffuse into the epitaxial layer to form an island of p- type material.

→ The SiO_2 layer is again formed on the wafer by blowing pure oxygen over the wafer. Thus, a p-n junction diode is formed on the substrate.



(i)



(ii)

(ii) Transistors :-

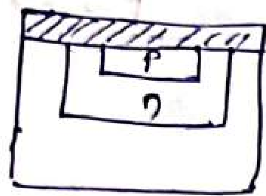
→ The steps used for fabricating the diode are carried out.

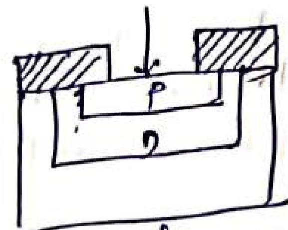
→ Then, a window is now formed at the centre of SiO_2 layer, thus exposing the p- epitaxial layer.

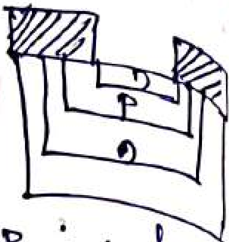
→ The pentavalent atoms diffuse into the epitaxial layer to form an island of n - type material.

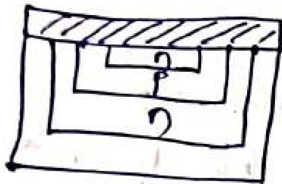
→ The SiO_2 layer is reformed over the wafer by passing pure oxygen.

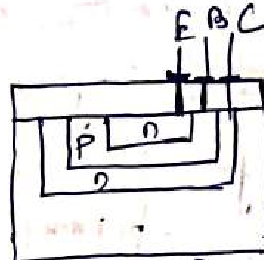
→ The terminals are processed by etching the SiO_2 layer at appropriate locations and depositing the metal at these locations.

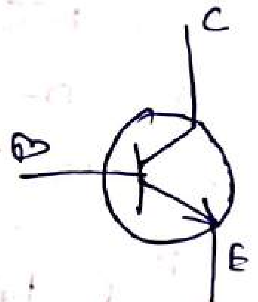






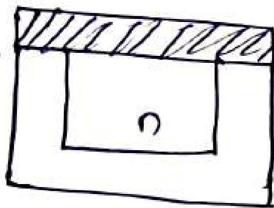


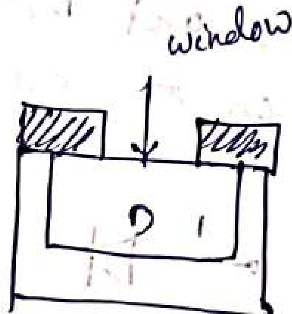


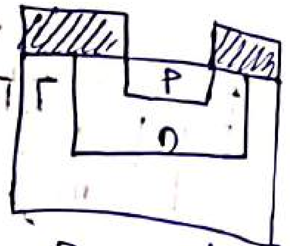


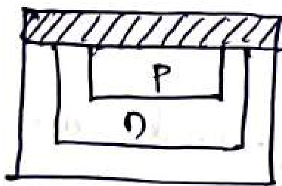
<iii>

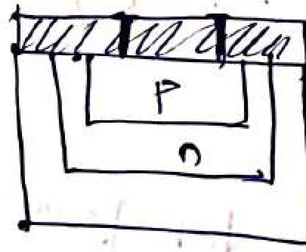
Resistors :

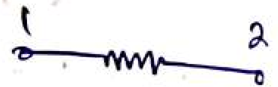












→ Initially, a n island is formed and sealed off as shown in the figure.

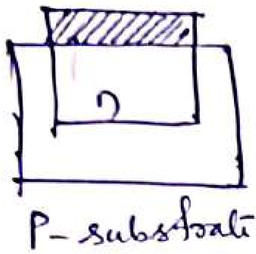
→ A window is now formed at the centre of SiO_2 layer thus exposing the n- epitaxial layer.

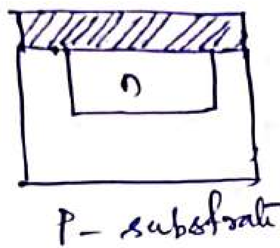
→ Then, a p-type material is diffused into the n-type area.

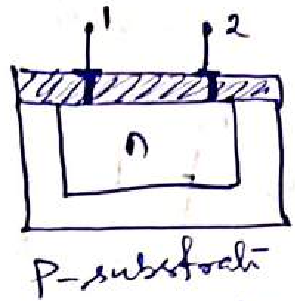
→ The SiO_2 layer is re-formed over the wafer by passing pure oxygen.

→ The terminals are processed by etching SiO_2 layer at two points above the P island and depositing the metal at these locations. Thus, can the resistor is integrated.

(iv) Capacitors :


P- substrate


P- substrate



P- substrate

→ The first step is to diffuse an n-type material into the substrate, which forms one plate of the capacitor.

→ Then SiO_2 layer is re-formed over the wafer by passing pure oxygen.

→ The SiO_2 layer formed acts as the dielectric of the capacitor.

→ The oxide layer is etched and terminal 1 is added.

Next a large metallic electrode is deposited on the SiO_2 layer and forms the second plate of the capacitor. The oxide layer is etched and terminal 2 is added. This gives an integrated capacitor.

Limitations of VLSI :

VLSI design faces limitations in scaling, manufacturing, design complexity, timing closure, and reliability, impacting the development and performance of integrated circuits.

→ Fabricating extremely small features with high precision and uniformity is difficult and expensive.

→ Designing complex VLSI circuits with millions or billions of transistors requires sophisticated design tools and methodologies.

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→ Meeting tight timing constraints in complex circuits can be a major challenge, requiring careful optimization and analysis.

→ Ensuring the long term reliability of VLSI devices crucial.

→ There is an inverse relationship between power dis[sipation] and propagation delay in logic circuits, which can be a challenge to optimize.

→ Developing VLSI devices is costly and time consuming process, requiring substantial investments in design tools, development platforms, and testing equipment.