DEPARTMENT OF COMPUTER SCIENCE ENGINEERING

Govt College of Engineering Kalahandi

Computer Organization and Architecture

Lab Manual

B.Tech., Semester -IV

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Experiment 1 a): Identification of Different Components of a PC

Aim

To identify various internal and external components of a computer system.

Theory

A computer system consists of motherboard, CPU, RAM, SMPS, storage devices, expansion cards, and peripheral devices.

Procedure

1. Open the cabinet carefully.
2. Identify motherboard, RAM, processor, HDD/SSD, and SMPS.
3. Observe peripheral ports and expansion slots.
4. Record specifications of each component.

Result

Different components of a PC were identified successfully.

Experiment 1 b): Assembling and Disassembling of a PC

Aim
To learn assembling and disassembling procedures of a computer.

Theory
PC assembly involves installing processor, RAM, storage devices, SMPS, and peripherals properly.

Procedure
5. Disconnect power supply.
6. Remove cabinet cover.
7. Detach RAM, HDD, SMPS carefully.
8. Reassemble all components properly.
9. Boot the system and verify.

Result
PC assembled and disassembled successfully.

Experiment 2: Study of SMPS with Single Output under Line Regulation

Aim
To study the working of SMPS and observe output voltage regulation.

Theory
SMPS converts AC input into regulated DC output efficiently.

Procedure
10. Connect SMPS trainer kit.
11. Apply AC input.
12. Measure output voltage using multimeter.
13. Vary input voltage and observe changes.

Result
Line regulation characteristics of SMPS were studied.

Experiment 3: Study of CPU Trainer Kit

AIM: Working of Computer Trainer

OBJECTIVE: To understand the working of Computer trainer.

PROCEDURE:

1. Connect the AC Supply to the Trainer kit.
2. Connect VGA connector of Monitor to the **VGA** slot of **"DISPLAY BLOCK"** of the trainer.
3. Set all the fault switches **FS-SW1 – FS-SW9** at **ON** Position.
4. Switch **ON** the power supply provided in the front end of the kit.
5. Press **"POWER ON"** button provided in the trainer.
6. Wait for few seconds till the system reached in free running mode and u will see the home screen appears on your monitor.
7. Now you can operate the Computer as per your need.

CONCLUSION:

Hence we have studied the working of computer trainer.

Experiment 4: Troubleshooting of Dot Matrix Printer

Aim
To study troubleshooting techniques for dot matrix printers.

Theory
Dot matrix printers use pins and ribbon mechanism for printing.

Procedure
14. Connect the printer module.
15. Check power and cable connections.
16. Simulate common faults like paper jam.
17. Rectify the fault and test printing.

Result
Printer troubleshooting performed successfully.

Experiment 5: IEEE 754 Floating Point Representation using C/C++

Aim

To implement IEEE 754 floating point representation.

Theory

IEEE 754 standard defines binary representation of floating-point numbers.

Procedure

18. Write a C/C++ program.
19. Input a floating-point number.
20. Convert number into binary representation.
21. Display sign, exponent, and mantissa.

Program/Code

```
#include<stdio.h>
int main() {
   float num;
   scanf("%f",&num);
   unsigned int *p=(unsigned int*)&num;
   for(int i=31;i>=0;i--)
      printf("%d",(*p>>i)&1);
   return 0;
}
```

Result

IEEE 754 representation displayed successfully.

Experiment 6: Signed Bit Multiplication using Booth's Algorithm

Aim
To perform signed multiplication using Booth’s Algorithm.

Theory
Booth’s Algorithm efficiently multiplies signed binary numbers.

Procedure
22. Initialize multiplicand and multiplier.
23. Check Q0 and Q-1 bits.
24. Perform add/subtract operation.
25. Apply arithmetic right shift repeatedly.

Result
Signed multiplication performed successfully.

Experiment 7: Study of Half Adder

Aim
To study and verify Half Adder operation.

Theory
Half Adder adds two binary digits and produces Sum and Carry.

Procedure
26. Connect XOR gate for Sum output.
27. Connect AND gate for Carry output.
28. Apply all possible inputs.
29. Verify outputs using truth table.

Truth Table

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Result
Half Adder verified successfully.

Experiment 8: Study of Full Adder

Aim
To study and verify Full Adder operation.

Theory
Full Adder adds three binary bits including carry input.

Procedure
30. Connect logic gates according to Full Adder circuit.
31. Apply all combinations of inputs.
32. Observe Sum and Carry outputs.
33. Verify with truth table.

Result
Full Adder verified successfully.

Experiment 9: Design of MUX, DEMUX & ALU using VHDL

Aim
To design digital circuits using VHDL.

Theory
VHDL is a hardware description language used for digital circuit design.

Procedure
34. Open Active VHDL software.
35. Write VHDL code for MUX/DEMUX/ALU.
36. Compile the code.
37. Simulate and verify outputs.

Program/Code
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux2to1 is
Port(A,B,S: in STD_LOGIC;
Y: out STD_LOGIC);
end mux2to1;

architecture Behavioral of mux2to1 is
begin
Y <= A when S='0' else B;
end Behavioral;
```

Result
Digital circuits designed successfully using VHDL.

Experiment 10: Assembly Language Program using 8086 Architecture

Aim

To study assembly language programming in 8086 microprocessor.

Theory

8086 is a 16-bit microprocessor with powerful instruction set.

Procedure

38. Open 8086 simulator.
39. Write assembly program.
40. Compile and execute.
41. Observe register values.

Program/Code

```
MOV AX,0005H
MOV BX,0003H
ADD AX,BX
HLT
```

Result

8086 assembly language program executed successfully.