# SUBJECT-BASIC ELECTRONICS ENGINEERING

## MODULE-I

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**Topic includes**

- **Construction and operation of p-n Junction Diode**
- **Construction and operation of Rectifier**
- **Zener Diode**
- **Bipolar Junction Transistor**

## 1. P-N JUNCTION DIODE

A ***p-n* junction** is formed by joining *p*-type and *n*-type semiconductors together in very close contact. The term *junction* refers to the boundary interface where the two regions of the semiconductor meet. If they were constructed of two separate pieces this would introduce a grain boundary, so *p-n* junctions are created in a single crystal of semiconductor by doping, for example, by ion implantation, diffusion of dopants, or by epitaxy (growing a layer of crystal doped with one type of dopant on top of a layer of crystal doped with another type of dopant). *p-n* junctions are elementary "building blocks" of almost all semiconductor electronic devices such as diodes, transistors, solar cells, LEDs, and integrated circuits. The regions near by the *p-n* interfaces lose their neutrality and become charged, forming the space charge region or depletion layer

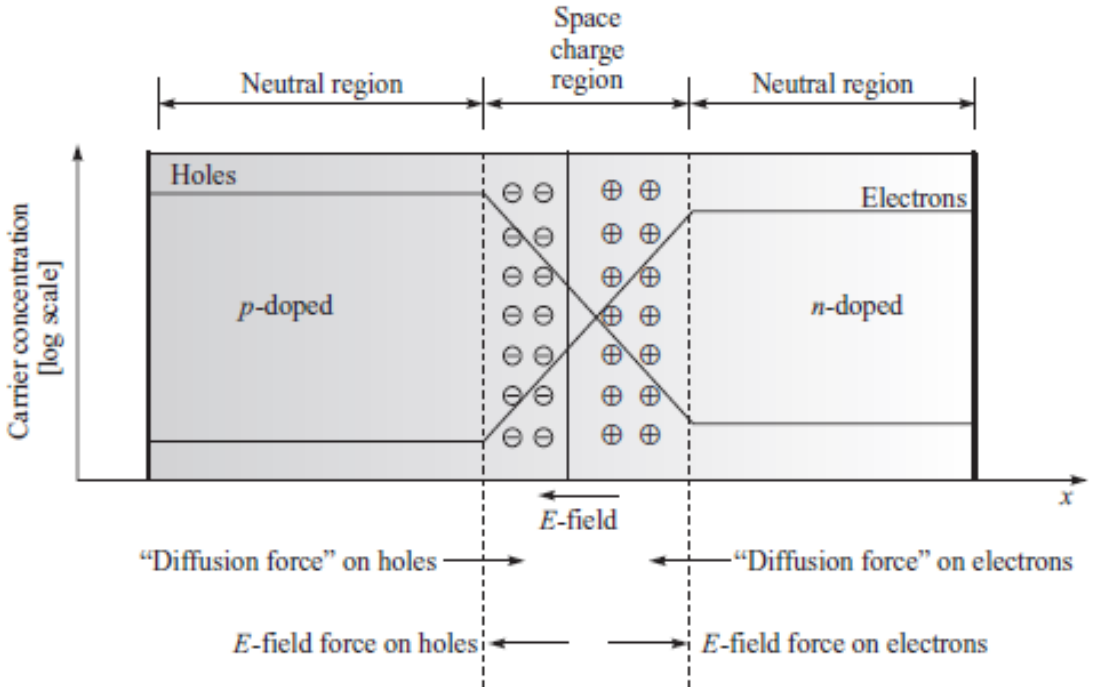



Fig.1. A p-n junction in thermal equilibrium with zero bias voltage applied

The electric field created by the space charge region opposes the diffusion process for both electrons and holes. There are two concurrent phenomena: the diffusion process that tends to generate more space charge, and the electric field generated by the space charge that tends to counteract the diffusion. The carrier concentration profile at equilibrium is shown in Fig.1. The

space charge region is a zone with a net charge provided by the fixed ions (donors or acceptors) that have been left uncovered by majority carrier diffusion. When equilibrium is reached, the charge density is approximated by the displayed step function. In fact, the region is completely depleted of majority carriers (leaving a charge density equal to the net doping level), and the edge between the space charge region and the neutral region is quite sharp. The space charge region has the same charge on both sides of the *p*-*n* interfaces, thus it extends farther on the less doped side.

## 2. FORWARD BIASING AND REVERSE BIASING

### *Forward Biasing:*

When external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow is called forward biasing. To apply forward bias, connect +ve terminal of the battery to *p*-type and –ve terminal to *n*-type as shown in Fig. 2. The applied forward potential establishes the electric field which acts against the field due to potential barrier. Therefore, the resultant field is weakened and the barrier height is reduced at the junction as shown in Fig. 2.2. Since the potential barrier voltage is very small, a small forward voltage is sufficient to completely eliminatethe barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit. Therefore, current flows in the circuit. This is called *forward current.*

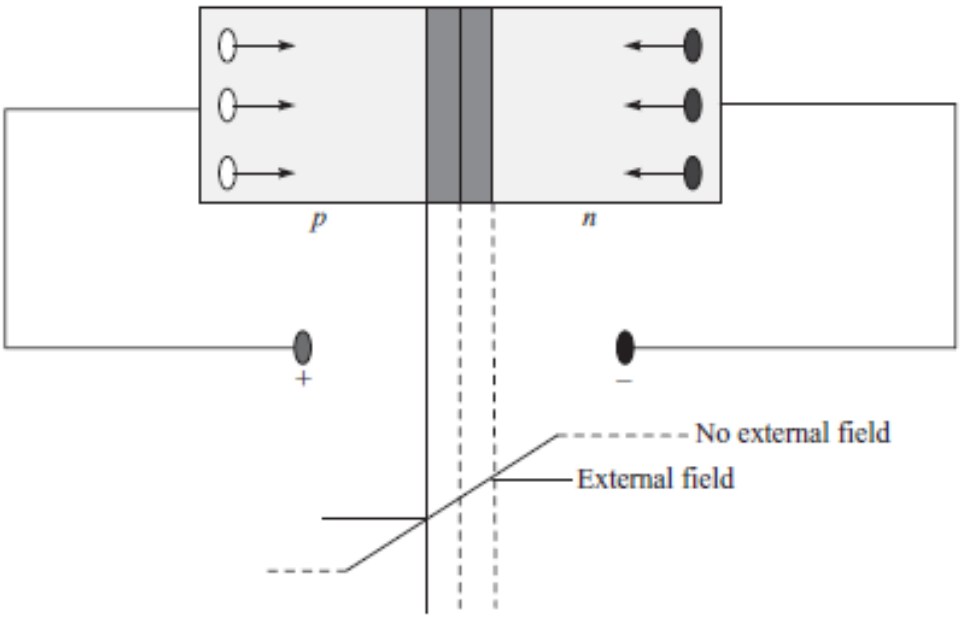



Fig. 2. Forward biasing of p-n junction

### *Reverse Biasing*

When the external voltage applied to the junction is in such a direction the potential barrier is increased it is called reverse biasing. To apply reverse bias, connect –ve terminal of the battery to *p*-type and +ve terminal to *n*-type as shown in Fig.3. The applied reverse voltage establishes an electric field which acts in the same

direction as the field due to potential barrier. Therefore, the resultant field at the junction is strengthened and the barrier height is increased as shown in Fig.3. The increased potential barrier prevents the flow of charge carriers across the junction. Thus, a high resistance path is established for the entire circuit and hence current does not flow.

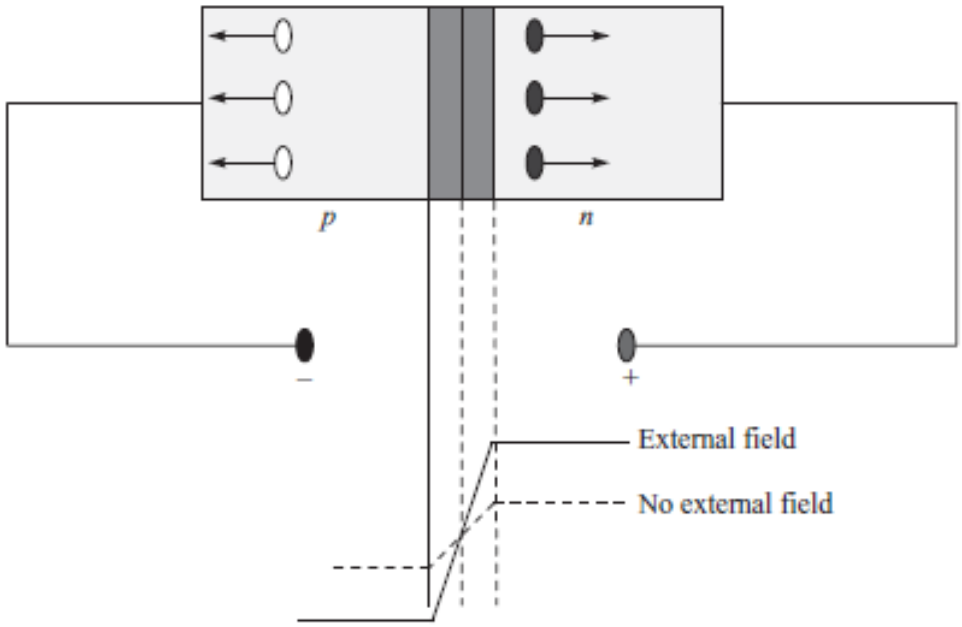



Fig. 3. Reverse biasing of p-n junction

## 3. VOLT-AMPERE (V-I ) CHARACTERISTICS OF P-N JUNCTION DIODE

The *V-I* characteristics of a semiconductor diode can be obtained with the help of the circuit shown in Fig. 4 (i). The supply voltage *V* is a regulated power supply, the diode is forward biased in the circuit shown. The resistor *R* is a current limiting resistor. The voltage across the diode is measured with the help of voltmeter and the current is recorded using an ammeter. By varying the supply voltage different sets of voltage and currents are obtained. By plotting these values on a graph, the forward characteristics can be obtained. It can be noted from the graph the current remains zero till the diode voltage attains the barrier potential. For silicon diode, the barrier potential is 0.7 V and for germanium diode, it is 0.3 V. The barrier potential is also called *knee voltage* or *cut-in voltage*. The reverse characteristics can be obtained by reverse biasing the diode. It can be noted that at a particular reverse voltage, the reverse current increases rapidly. This voltage is called *breakdown voltage*.

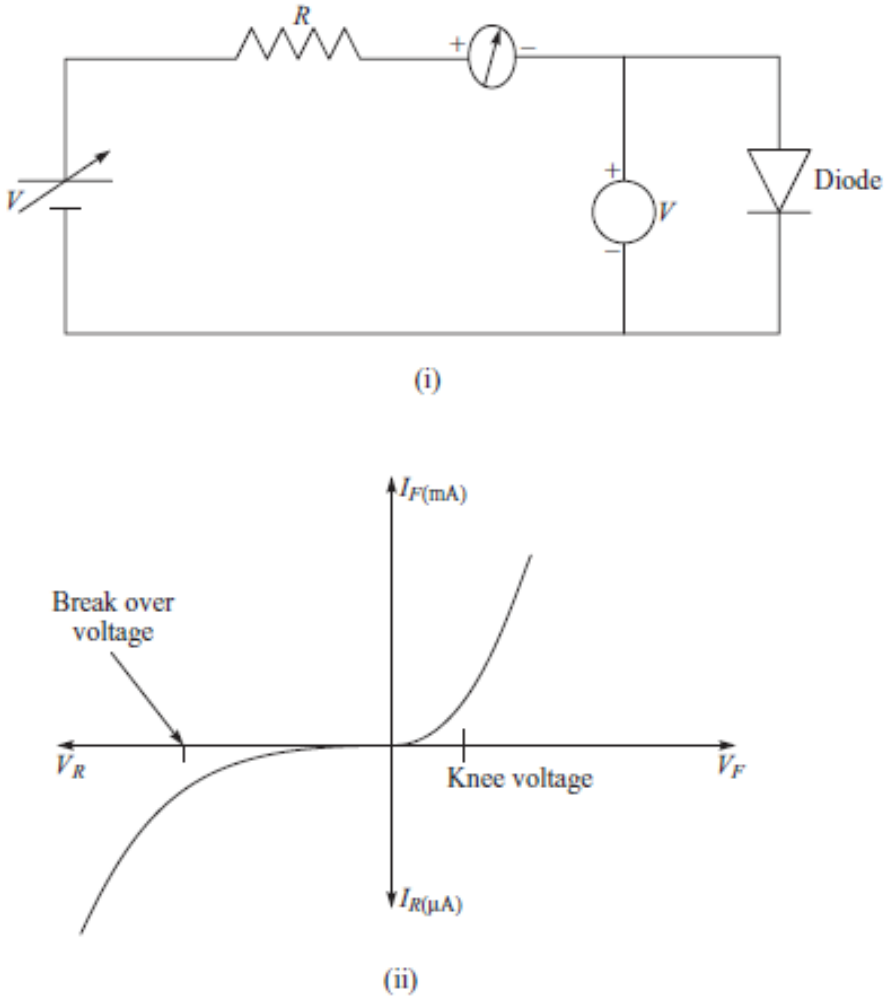



Fig. 4 V-I characteristics of p-n junction diode (i) circuit diagram; (ii) charactristics

## 4. DIODE CURRENT EQUATION

The current in a diode is given by the diode current equation

$$I = I_o(e^{V/\eta V_T} - 1)$$

where, $I$ = Diode current
$I_o$ = Reverse saturation current
$V$ = Diode voltage
$\eta$ = Semiconductor constant
= 1 for Ge
= 2 for Si.

$V_T$ = Voltage equivalent of temperature = $T/11{,}600$ (temperature $T$ is in kelvin)

**Note:** If the temperature is given in °C then it can be converted to kelvin with the help of the following relation, °C + 273 = K

## 5. DIODE EQUIVALENT CIRCUIT

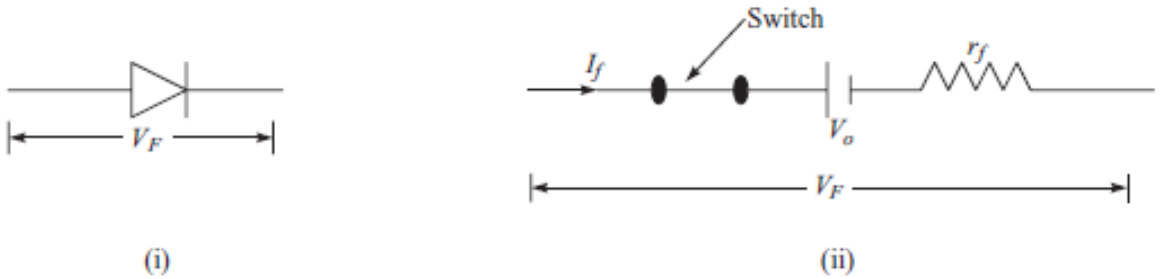



Fig. 5. Diode equivalent circuit. (i) Symbol (ii) equivalent circuit

The forward current $I_f$ flowing through the diode causes a voltage drop in its internal resistance, $r_f$. Therefore, the forward voltage $V_F$ applied across the actual diode has to overcome

1. potential barrier $V_o$
2. internal drop $I_f r_f$

$$V_f = V_o + I_f r_f$$

For silicon diode $V_o$ = 0.7 V whereas for germanium diode $V_o$ = 0.3 V.

For ideal diode $r_f$ = 0.

## Basic Definitions

### *Knee Voltage or Cut-in Voltage*

It is the forward voltage at which the diode starts conducting.

### *Breakdown Voltage*

It is the reverse voltage at which the diode (*p-n* junction) breaks down with a sudden rise in reverse current.

### *Peak-inverse Voltage (PIV)*

It is the maximum reverse voltage that can be applied to a *p-n* junction without causing damage to the junction. If the reverse voltage across the junction exceeds its peak inverse voltage, then the junction exceeds its peak-inverse voltage, and the junction gets destroyed because of excessive heat.

***Maximum Forward Current***

It is the maximum instantaneous forward current that a *p-n* junction can conduct without damaging the junction. If the forward current is more than the specified rating then the junction gets destroyed due to overheating.

## 6. VOLT-AMPERE (*V-I*) C HARACTERISTICS OF IDEAL DIODE

Diode permits only unidirectional conduction. It conducts well in forward direction and poorly in reverse direction. It would have been ideal if a diode acted as a perfect conductor (with zero voltage across it) when forward-biased, and as a perfect insulator (with no current through it) when reverse-biased. The *V-I* characteristics of such an ideal diode would be as shown in Fig. 6. An ideal diode acts like an automatic switch. When the current tries to flow in the forward direction, the switch is closed. On the other hand, when the current tries to flow in the reverse direction, the switch is open.

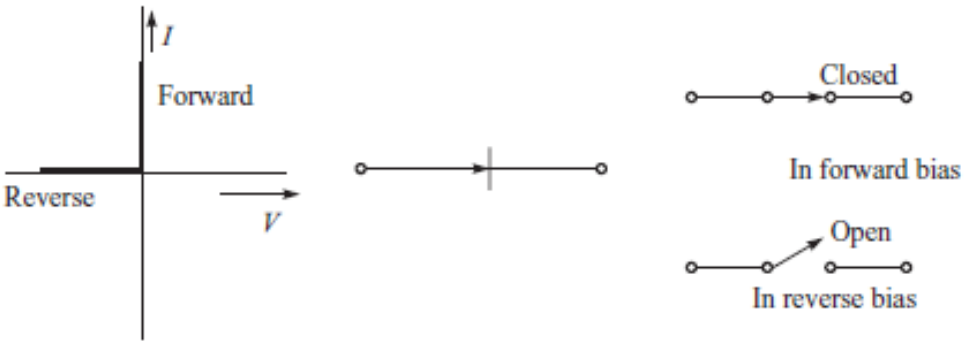



Fig. 6.

## 7. STATIC AND DYNAMIC RESISTANCE OF A DIODE

***DC or Static Resistance***

When diode is forward biased, it offers a definite resistance in the circuit. This resistance is known as dc resistance or static resistance ($R_F$). It is simply the ratio of the dc voltage ($V_D$) across the diode to the dc current ($I_D$) flowing through it as shown in Fig.7.

$$R_F = \frac{V_D}{I_D}$$

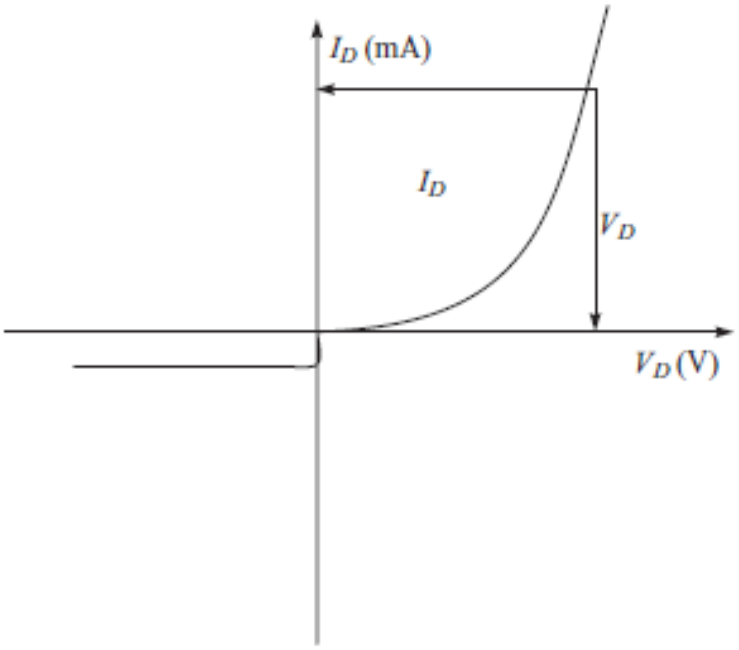



Fig. 7. Determination of dc resistance of a diode at a specific operating point

### *AC or Dynamic Resistance*

The ac or dynamic resistance of a diode, at a particular dc voltage, is equal to the reciprocal of the slope of the characteristics at that point, as shown in Fig. 8.

$$r_f = \frac{\Delta V_D}{\Delta I_D}$$

$\Delta V_D$= change in voltage

$\Delta I_D$= change in current

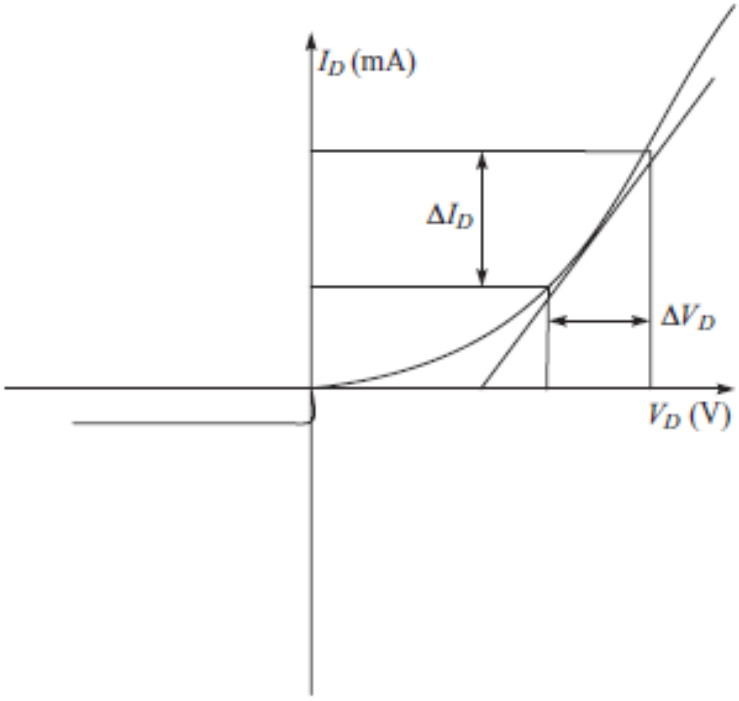



Fig. 8. Determination of ac resistance of a diode at a specific operating point

## 8. HALF-WAVE RECTIFIER

The circuit diagram of a half-wave rectifier is shown in Fig. 9 along with the *I*/*P* and *O*/*P* waveforms.

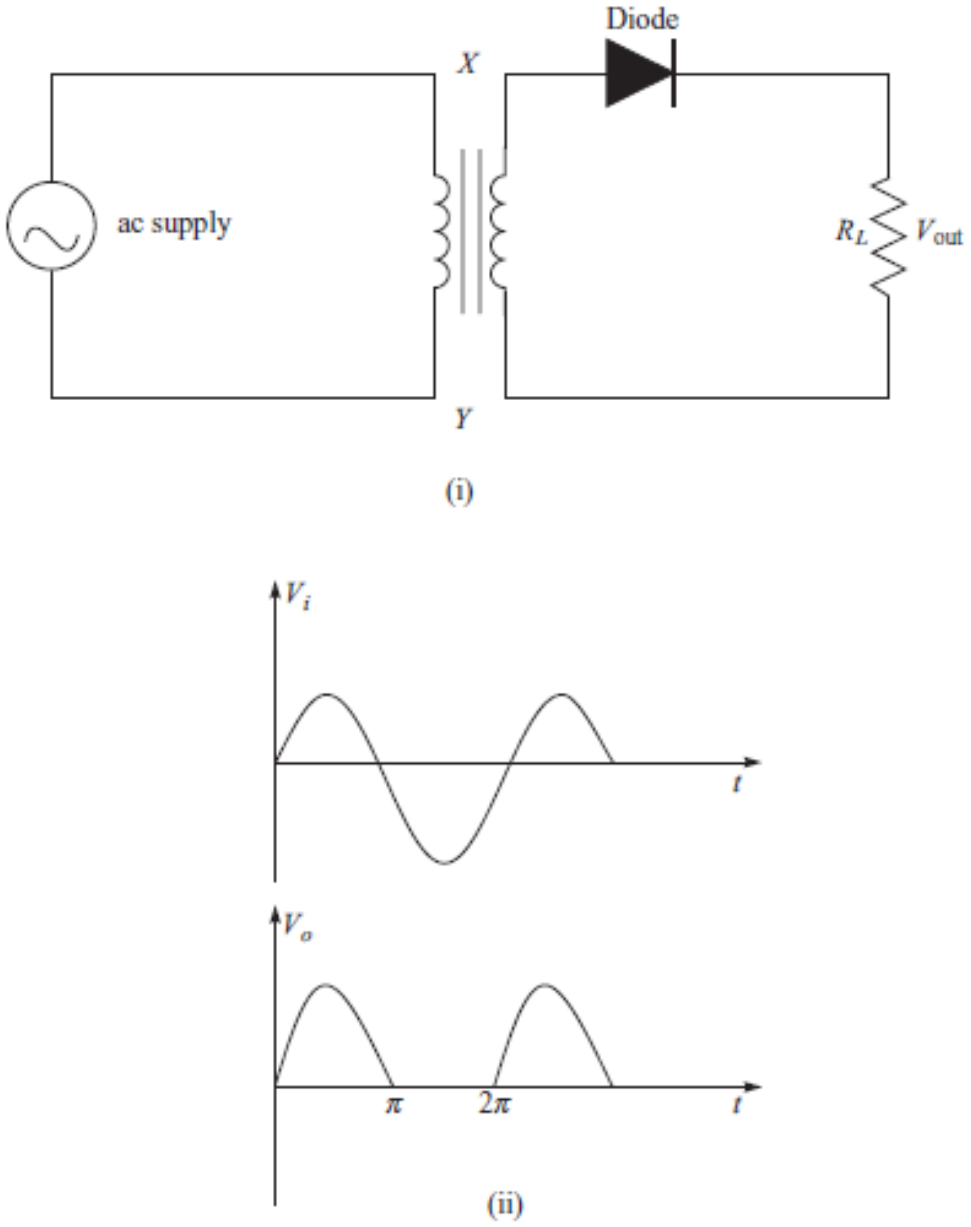



Fig. 9

The transformer is employed in order to step-down the supply voltage and also to prevent from shocks. The diode is used to rectify the ac signal while the pulsating dc is taken across the load resistor *RL*. During the +ve half-cycle, the end *X* of the secondary is +ve and end *Y* is –ve. Thus, forward biasing the diode. As the diode is forward biased, the current flows through the load *RL* and a voltage is developed across it. During the –ve half-cycle the end *Y* is +ve and

end *X* is –ve thus, reverse biasing the diode. As the diode is reverse biased there is no flow of current through *RL* thereby the output voltage is zero.

## *Efficiency of a Rectifier*

The ratio of dc power to the applied input ac power is known as rectifier efficiency.

Rectifier efficiency $\eta = \dfrac{dc\ power\ output}{input\ ac\ power}$

Let $V = Vm \sin \theta$ be the voltage across the secondary winding
$r_f$ = diode resistance
$R_L$ = load resistance

### *dc Power*

$$I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i \cdot d\theta = \frac{1}{2\pi}\int_0^{\pi} \frac{V_m \sin\theta}{r_L + R_L} d\theta$$

$$= \frac{V_m}{2\pi (r_f + R_L)}\int_0^{\pi} \sin\theta \, d\theta$$

$$= \frac{2V_m}{2\pi (r_f + R_L)} = \frac{I_m}{\pi}$$

dc power $P_{dc} = I_{dc}^2 \times R_L$

$$= \left(\frac{I_m}{\pi}\right)^2 \times R_L$$

***ac Power Input***

The ac power input is given by $P_{ac} = I_{rms}^2 (r_f + R_L)$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d\theta}$$

Squaring both sides, we get

$$I_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} i^2 d\theta$$

But $i = I_m \sin\theta$

$$I_{rms}^2 = \frac{1}{2\pi}\int_0^{\pi} (I_m \sin\theta)^2 d\theta \text{ (current flows through diode only for duration 0 to } \Pi)$$

$$I_{rms}^2 = \frac{I_m^2}{4}$$

$$I_{rms} = \frac{I_m}{2}$$

$$\therefore \quad P_{ac} = \left(\frac{I_m}{2}\right)^2 (r_f + R_L)$$

$$\therefore \quad \eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{I_m}{\pi}\right)^2}{\left(\frac{I_m}{2}\right)^2} \times \frac{R_L}{(r_f + R_L)}$$

$$\eta = \frac{0.406}{1 + \frac{r_f}{R_L}}$$

## 9. FULL-WAVE RECTIFIER

Full wave Rectifier of two types

(i) Centre tapped full-wave rectifier

(ii) Bridge fullwave rectifier

***(i) Centre tapped full-wave rectifier***

The circuit diagram of a centre tapped full-wave rectifier is shown in Fig. 10. It employs two diodes and a centre tap transformer. The ac signal to be rectified is applied to the primary of the transformer and the dc output is taken across the load, $R_L$. During the +ve half-cycle end *X* is +ve and end *Y* is –ve. This makes diode $D_1$ forward biased and thus a current $i1$ flows through

it and load resistor $R_L$. Diode $D_2$ is reverse biased and the current $i_2$ is zero. During the –ve half-cycle end $Y$ is +ve and end $X$ is –ve. Now diode $D_2$ is forward biased and thus a current $i_2$ flows through it and load resistor $R_L$. Diode $D_1$ is reversed and the current $i_1 = 0$.

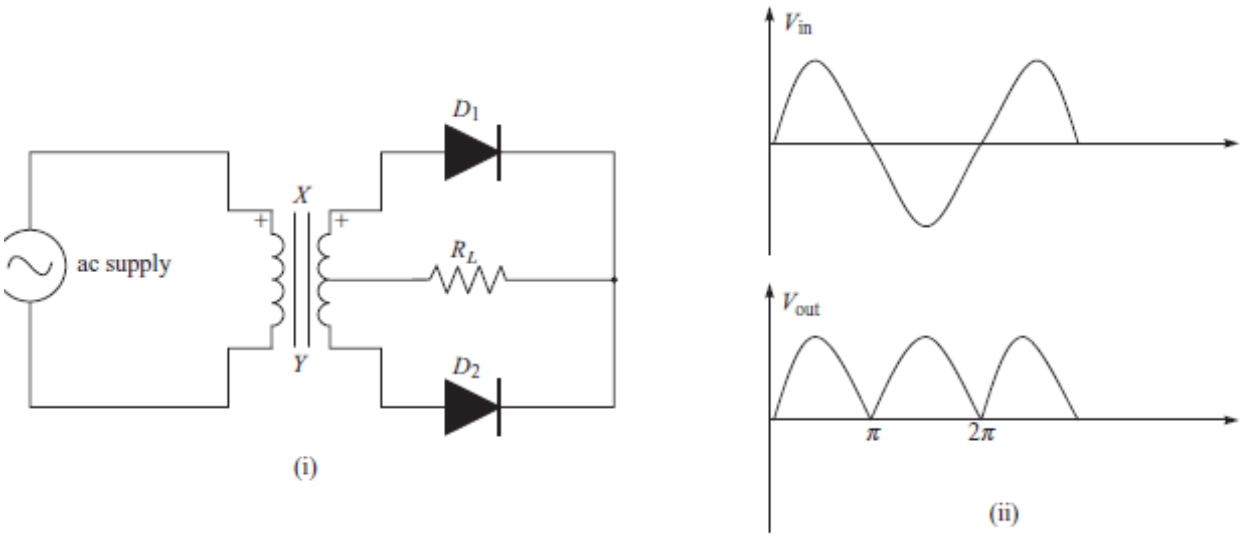


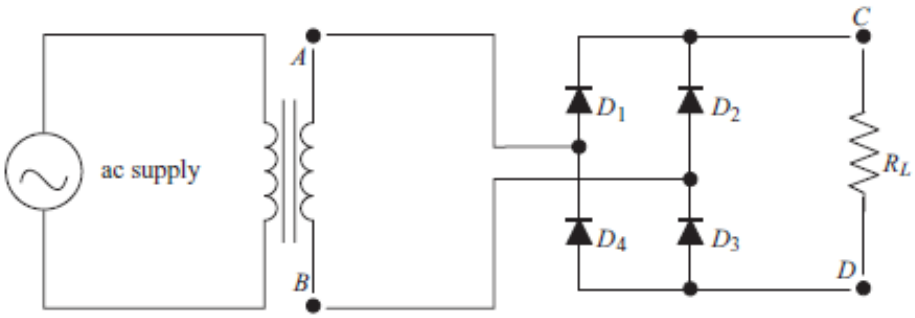

Fig.10. Centre tapped full-wave rectifier (i) circuit diagram; (ii) input and output waveforms

***(ii) Bridge rectifier***

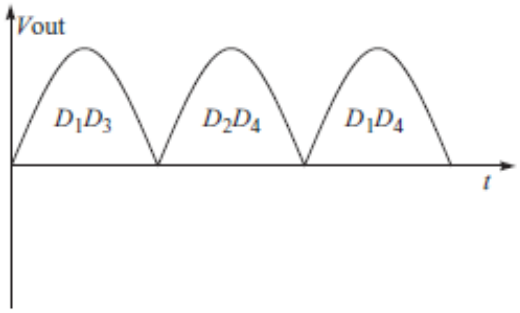
The circuit diagram of a bridge rectifier is shown in Fig. 11. It uses four diodes and one transformer.

During the +ve half-cycle, end $A$ is +ve and end $B$ is –ve thus diodes $D_1$ and $D_3$ are forward bias while diodes $D_2$ and $D_4$ are reverse biased thus a current flows through diode $D_1$, load $R_L$ ($C$ to $D$) and diode $D_3$.

During the –ve half-cycle, end $B$ is +ve and end $A$ is –ve thus diodes $D_2$ and $D_4$ are forward biased while the diodes $D_1$ and $D_3$ are reverse biased. Now the flow of current is through diode $D_4$ load $R_L$ ($D$ to $C$) and diode $D_2$. Thus, the waveform is same as in the case of centre-tapped full-wave rectifier.




(i)




(ii)

**Fig. 11.** Centre tapped full-wave rectifier (i) circuit diagram; (ii) output waveform

## *Efficiency of full-wave rectifier*

Let $V = V_m \sin\theta$ be the voltage across the secondary winding
$I = I_m \sin\theta$ be the current flowing in secondary circuit
$r_f$ = diode resistance
$R_L$ = load resistance

dc power output

$$P_{dc} = I_{dc}^2 R_L$$

$$I_{dc} = I_{av} = 2\frac{1}{2\pi}\int_0^{\pi} i \cdot d\theta$$

$$I_{av} = 2\frac{1}{2\pi}\int_0^{\pi} I_m \sin\theta \cdot d\theta$$

$$I_{av} = \frac{2I_m}{\pi}$$

$\therefore$

$$P_{dc} = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

input ac power

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

$$I_{rms} = \sqrt{2\frac{1}{2\pi}\int_0^{\pi} i^2 d\theta}$$

Squaring both sides, we get

$$I_{rms}^2 = \frac{1}{\pi}\int_0^{\pi} i^2 d\theta$$

$$I_{rms}^2 = \frac{1}{\pi}\int_0^{\pi} (I_m \sin\theta)^2 d\theta$$

$$I_{rms}^2 = \frac{I_m^2}{2}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$P_{ac} = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)$$

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{2I_m}{\pi}\right)^2}{\left(\frac{I_m}{\sqrt{2}}\right)^2} \times \frac{R_L}{(r_f + R_L)}$$

$$\eta = \frac{0.812}{1 + \frac{r_f}{R_L}}$$

The efficiency will be maximum if $r_f$ is negligible as compared to $R_L$.

Hence, maximum efficiency = 81.2%

This is double the efficiency due to half-wave rectifier. Therefore, a full-wave rectifier is twice as effective as a half-wave rectifier.

## *Ripple Factor*

The pulsating output of a rectifier consists of dc component and ac component (also known as ripple). The effectiveness of a rectifier depends on the magnitude of ac component in the output : the smaller this component, the more effective is the rectifier.

Ripple factor (r) is defined as it is the ratio of rms value of ac component to the dc component in the rectifier output.

$$r = \frac{I_{ac}}{I_{dc}}$$

### *Ripple Factor for halfwave rectifier*

By definition the effective (i.e., rms) value of total load current is given by

$$I_{rms}^2 = I_{ac}^2 + I_{dc}^2$$

$$I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2}$$

where $I_{dc}$ = value of dc component

$I_{ac}$ = rms value of ac component

Divide both RHS and LHS by $I_{dc}$, we get

$$\frac{I_{ac}}{I_{dc}} = \frac{1}{I_{dc}}\sqrt{I_{rms}^2 - I_{dc}^2}$$

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

For half-wave rectification, $I_{rms} = \frac{I_m}{2}$ and $I_{dc} = \frac{I_m}{\pi}$

So, the ripple factor (r) of half-wave rectifier is 1.21.

### *Ripple Factor for Full-wave Rectification*

For full-wave rectification,

$I_{rms} = \frac{I_m}{\sqrt{2}}$ and $I_{dc} = \frac{2I_m}{\pi}$

So, the ripple factor (r) of full-wave rectifier is 0.48.

## 10. COMPARISON OF RECTIFIERS

| Particulars | Half-wave rectifier | Centre-tapped full-wave rectifier | Bridge rectifier |
|---|---|---|---|
| 1. No. of diodes | 1 | 2 | 4 |
| 2. $I_{dc}$ | $I_m/\Pi$ | $2I_m/\Pi$ | $2I_m/\Pi$ |
| 3. $V_{dc}$ | $V_m/\Pi$ | $2V_m/\Pi$ | $2V_m/\Pi$ |
| 4. $I_{rms}$ | $I_m/2$ | $I_m/\sqrt{2}$ | $I_m/\sqrt{2}$ |
| 5. Efficiency | 40.6% | 81.2% | 81.2% |
| 6. PIV | $V_m$ | $2V_m$ | $V_m$ |
| 7. Ripple factor | 1.21 | 0.48 | 0.48 |

## Zener Diode

The Zener diode can be defined as; it is a special kind of diode when we compare with other diodes. The flow of current in this diode will be in a forward direction or in reverse direction. The Zener diode includes an individual and heavily doped PN-junction, which is intended to perform in the reverse bias direction when a particular voltage is reached. This diode contains a reverse breakdown voltage for current conducting as well as continuous operation in the mode of reverse bias without getting smashed. In addition, the voltage drop at the diode will remain stable over an extensive voltages range, and one of the main characteristics will make this diode suitable for utilizing in voltage regulation.

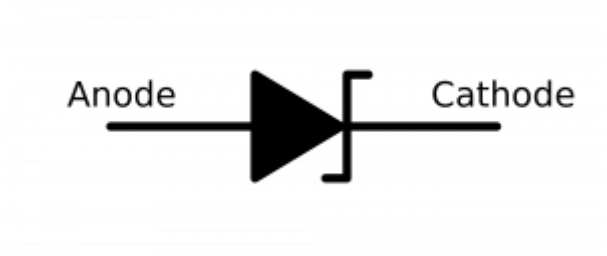



Fig.1. Symbol of zener diode.

## Zener Diode V-I Characteristics

The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the V-I characteristics curve as shown in Fig. 2., we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode.

This voltage remains almost constant even with large changes in current providing the zener diodes current remains between the breakdown current $I_{Z(min)}$ and its maximum current rating $I_{Z(max)}$.

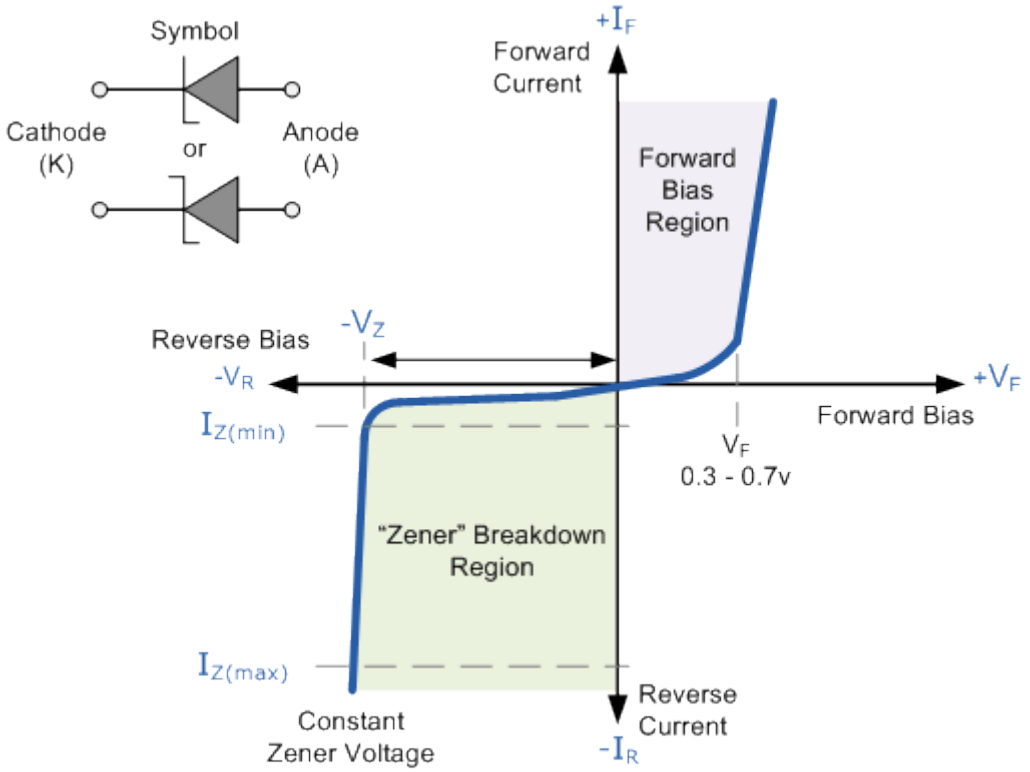



Fig. 2. V-I charactristics of zener diode.

This ability of the zener diode to control itself can be used to great effect to regulate or stabilise a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important characteristic of the zener diode as it can be used in the simplest types of voltage regulator applications.

The function of a voltage regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or variations in the load current. A zener diode will continue to regulate its voltage until the diodes holding current falls below the minimum $I_{Z(min)}$ value in the reverse breakdown region

## Zener Breakdown

The Zener breakdown mainly occurs because of a high electric field. When the high electric-field is applied across the PN junction diode, then the electrons start flowing across the PN-junction. Consequently, expands the little current in the reverse bias.

When the electron moving enhances beyond the diode rated capacity, then the avalanche breakdown will occur to break the junction. Therefore, the flow of current in the diode is incomplete the diode will not damage the PN-junction. However, avalanche breakdown will damage the junction.

**Zener Breakdown vs Avalanche Breakdown**

- The doping of the Zener is heavy whereas the avalanche is low.
- The reverse potential of the Zener is low whereas the avalanche is high.
- The temperature coefficient of the Zener is negative whereas the avalanche is positive.
- The Ionization of the Zener is due to Electric field whereas the avalanche is the collision.
- The temperature coefficient of the Zener is negative whereas the avalanche is positive.

## Zener Diode as Voltage Regulator

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. 1. The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply.

***$V_i$ and R Fixed***

The simplest of Zener diode regulator networks appears in Fig. 1 . The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

**Step 1. Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.**

Applying step 1 to the network of Fig. 1 results in the network of Fig. 2., Applying voltage divider rule, which results in

$$V = V_L = \frac{R_L V_i}{R + R_L} \quad (1)$$

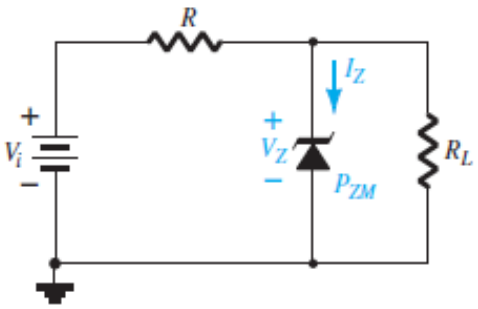



Fig. 1. Basic Zener regulator

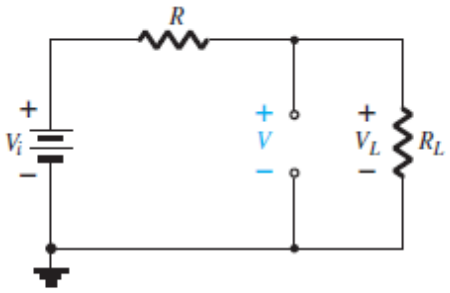



Fig. 2. Determining the state of the Zener diode

If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted.

If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

**Step 2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.**

For the network of Fig. 1. , the "on" state will result in the equivalent network of Fig. 3. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2}$$

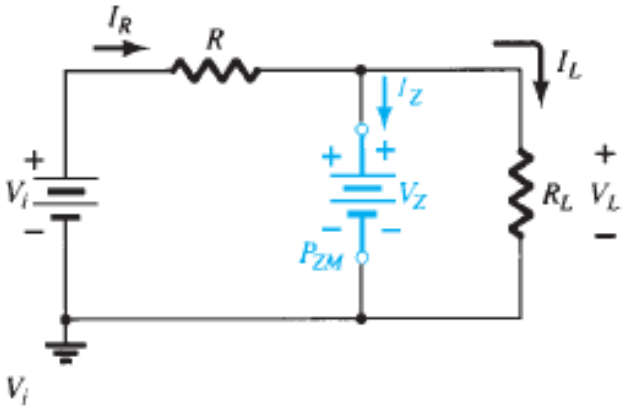



Fig. 3. Substituting the Zener equivalent for the "on"situation.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

$$I_Z = I_R - I_L \tag{3}$$

where

$$I_L = V_L / R_L \text{ and } I_R = V_R / R = (V_i - V_L) / R$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{4}$$

it is particularly important to realize that the first step was employed only to determine the state of the Zener diode. If the Zener diode is in the "on" state, the voltage across the diode is not $V$ volts. When the system is turned on, the Zener diode will turn on as soon as the voltage across the Zener diode is $V_Z$ volts. It will then "lock in" at this level and never reach the higher level of $V$ volts.

***Fixed $V_i$ , Variable $R_L$***

Due to the offset voltage $V_Z$ , there is a specific range of resistor values (and therefore load current) that will ensure that the Zener is in the "on" state. Too small a load resistance $R_L$ will result in a voltage $V_L$ across the load resistor less than $V_Z$ , and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.112 that will turn the Zener diode on, simply calculate the value of $R_L$ that will result in a load voltage $V_L = V_Z$ . That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for $R_L$ , we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} \tag{5}$$

Any load resistance value greater than the $R_L$ obtained from Eq. (5) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its $V_Z$ source equivalent. The condition defined by Eq. (5) establishes the minimum $R_L$ , but in turn specifies the maximum $I_L$ as

$$I_{L_{max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{min}}} \tag{6}$$

Once the diode is in the "on" state, the voltage across $R$ remains fixed at

$$V_R = V_i - V_Z \tag{7}$$

and $I_R$ remains fixed at

$$I_R = \frac{V_R}{R} \tag{8}$$

The Zener current

$$I_Z = I_R - I_L \tag{9}$$

resulting in a minimum $I_Z$ when $I_L$ is a maximum and a maximum $I_Z$ when $I_L$ is a minimum value, since $I_R$ is constant. Since $I_Z$ is limited to $I_{ZM}$ as provided on the data sheet, it does affect the range of $R_L$ and therefore $I_L$ . Substituting $I_{ZM}$ for $I_Z$ establishes the minimum $I_L$ as

$$I_{L_{min}} = I_R - I_{ZM} \tag{10}$$

and the maximum load resistance as

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}} \tag{11}$$

***Fixed $R_L$ , Variable $V_i$***

For fixed values of $R_L$ in Fig. 1. , the voltage $V_i$ must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = Vi_{min}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} \tag{12}$$

The maximum value of $V_i$ is limited by the maximum Zener current $I_{ZM}$ . Since $I_{ZM} = I_R - I_L$ ,

$$I_{R_{max}} = I_{ZM} + I_L \tag{13}$$

Since $I_L$ is fixed at $V_Z / R_L$ and $I_{ZM}$ is the maximum value of $I_Z$ , the maximum $V_i$ is defined by

$$Vi_{max} = V_{Rmax} + V_Z$$

$$V_{i_{max}} = I_{R_{max}} R + V_Z \tag{14}$$

# SUBJECT-BASIC ELECTRONICS ENGINEERING

# TOPIC-BIPOLAR JUNCTION TRANSISTOR

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# Bipolar Junction Transistor (BJT)

A bipolar junction transistor is a three layer semiconductor device which is consisting of two P layer and a N layer or two N layer with a P layer. A N layer is sandwiched between two P layer known as PNP transistor and similarly, if a P layer is sandwich between two N layer called as NPN transistor. The BJT consists of three terminal named as base (B), emitter (E) and collector (C).

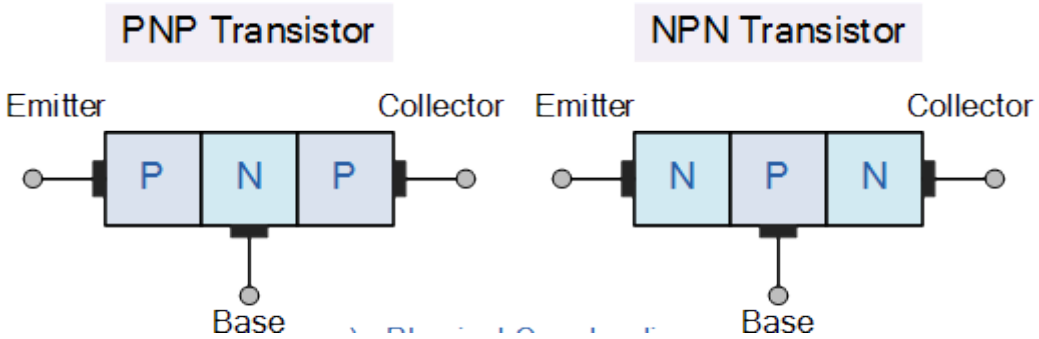


Fig.1. PNP and NPN transistor.


Fig. 2. Symbol of BJT: (a) PNP; (b) NPN.

The width and doping level of the base, emitter and collector are compares as:

Width: Base < Emitter < Collector

Doping : Emitter > Collecor > Base

The width of the collector layer is large as compared to based and emitter and the doping is high in emitter layer as compared to other two . The abbreviation BJT, from bipolar junction transistor, is often applied to this three-terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material.

## TRANSISTOR OPERATION

The basic arrangement with different bias volatge for npn and pnp transistor is shown in Fig. 4. Now, we will describe the operation of the pnp transistor as per the diagram depicted in Fig. 4a .The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig.5a the *pnp* transistor has been redrawn without the base-to collector bias. This is similar to the forward biasing of p-n junction diode. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p* - to the *n* -type material.

Let us now remove the base-to-emitter bias of the pnp transistor of Fig. 4a as shown in Fig. 5b . This is similar to the forward biasing of p-n junction diode. The depletion region has been expand in width due to the reverse bias voltage. The flow of majority carriers is zero, resulting in only a minority carriers flow.

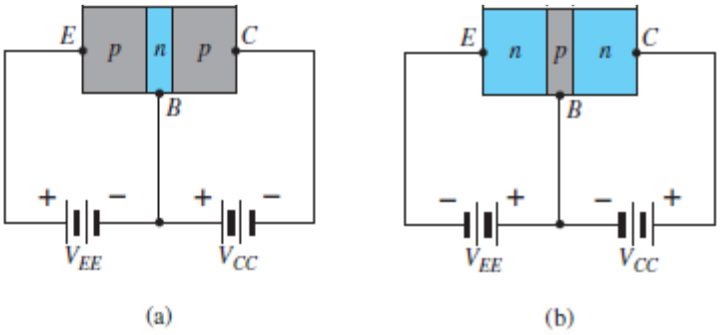


Fig. 4. Types of transistor: (a) pnp; (b) npn

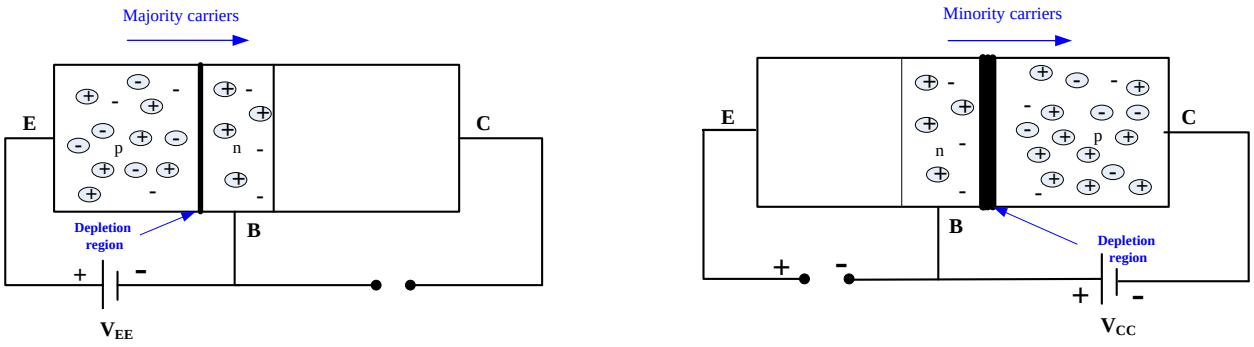


Fig. 5. Biasing of a transistor: (a) forward biased; (b) reverse biased.

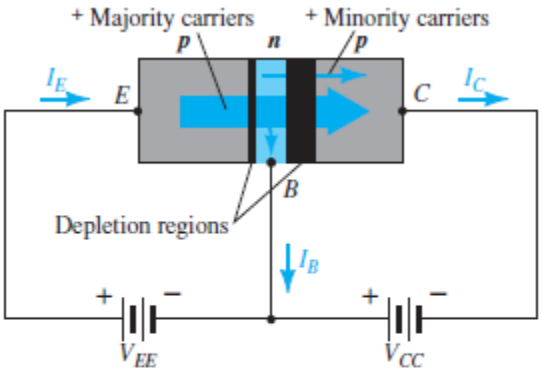


Fig. 6. Majority and minority carrier flow of a pnp transistor.

In Fig.6 both biasing potentials have been applied to a *pnp* transistor, with the resulting majority- and minority-carrier flows indicated. As indicated in Fig.6 , a large number of majority carriers will diffuse across the forward biased *p–n* junction into the *n* -type material. Since the sandwiched *n* -type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal. The magnitude of thebase current is typically on the order of microamperes, as compared to milliamperes for theemitter and collector currents. The larger number of these majority carriers will diffuse acrossthe reverse-biased junction into the *p* -type material connected to the collector terminal as indicatedin Fig.6 . All the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig.6 .

Applying Kirchhoff's current law to the transistor of Fig.6 as if it were a single node,we obtain

$$\boldsymbol{I_E = I_C + I_B}$$

So, emitter current is the sum of the collector and base currents.

The collector current, however, comprises two components–the majority and the minority carriers as indicated in Fig. 6 . The minority-current component is called the leakage current and is given the symbol $I_{CO}$ ($I_C$ current with emitter terminal open). The collector current, therefore, is determined in total by

$$\boldsymbol{I_C = I_{C\text{majority}} + I_{CO\text{minority}}}$$

$I_C$ is measured in milliamperes and $I_{CO}$ is measured in microamperes or nanoamperes. $I_{CO}$ , like $I_s$ for a reverse-biased diode.

## COMMON-BASE CONFIGURATION

The common base configuration with *pnp* and *npn* transistors is shown in Fig. 7. The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential. The arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.

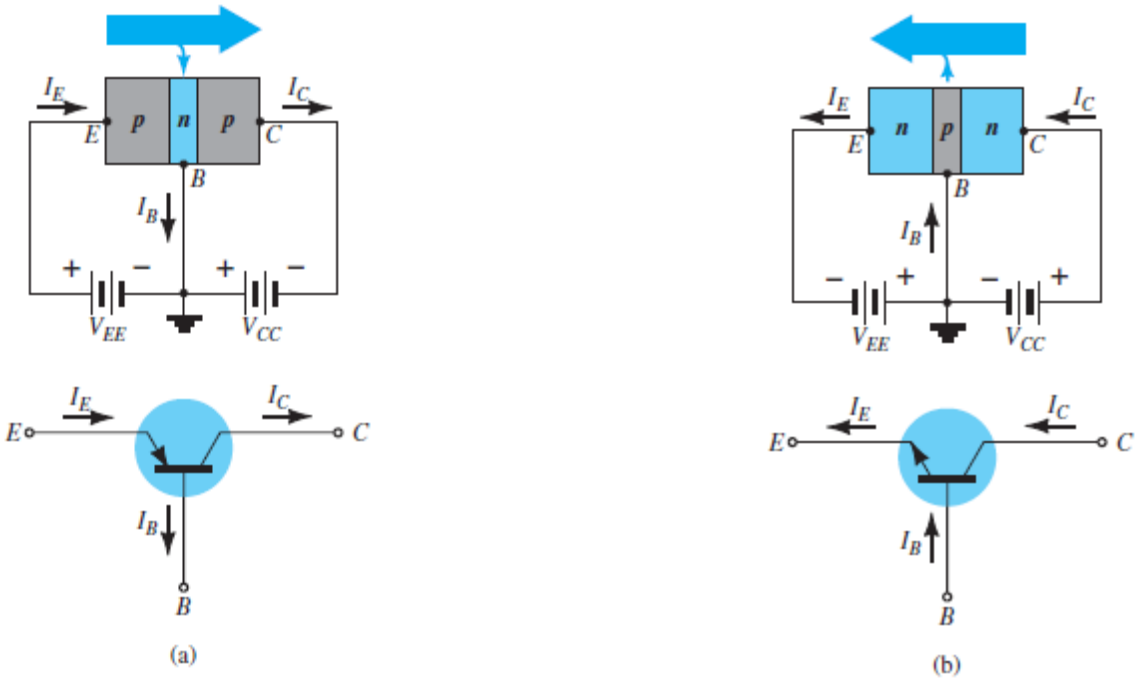


Fig. 7. Common base configuration: (a) pnp transistor; (b) npn transistor

### Input Characteristics

The input charactristics of the common base transistor configuration is depicted in Fig.8. The input set for the common-base amplifier as shown in Fig. 8 relates an input current ($I_E$) to an input voltage ($V_{BE}$) for various levels of output voltage ($V_{CB}$). The input characteristics of Fig.8 reveal that for fixed values of collector voltage ($V_{CB}$), as the base-to-emitter voltage increases, the emitter current increases in a manner that closely resembles the diode characteristics. In fact, increasing levels of $V_{CB}$ have such a small effect on the characteristics that as a first approximation the change due to changes in $V_{CB}$ can be ignored. once a transistor is in the "on" state, the base-to-emitter voltage will be assumed to be the following:

$$V_{BE} \cong 0.7\ V$$

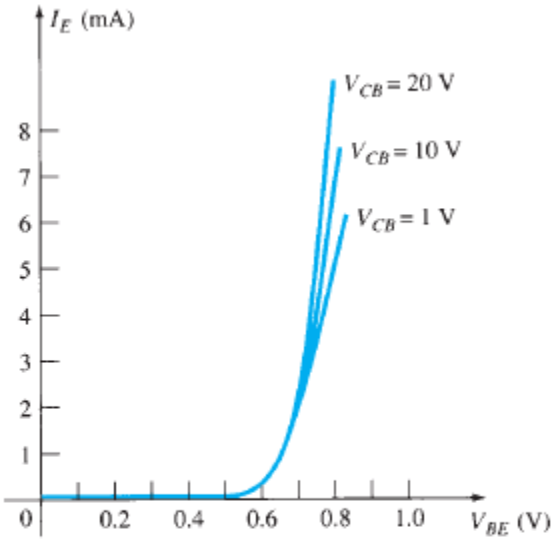


Fig. 8. Input characteristics of common base silicon amplifier.

**Output Characteristics**

The output set relates an output current ($I_C$) to an output voltage ($V_{CB}$) for various levels of input current ($I_E$) as shown in Fig. 9 . The output or collector set of characteristics has three basic regions of interest, as indicated in Fig. 9 : the active , cutoff , and saturation regions. The active region is the region normally employed for linear (undistorted) amplifiers.

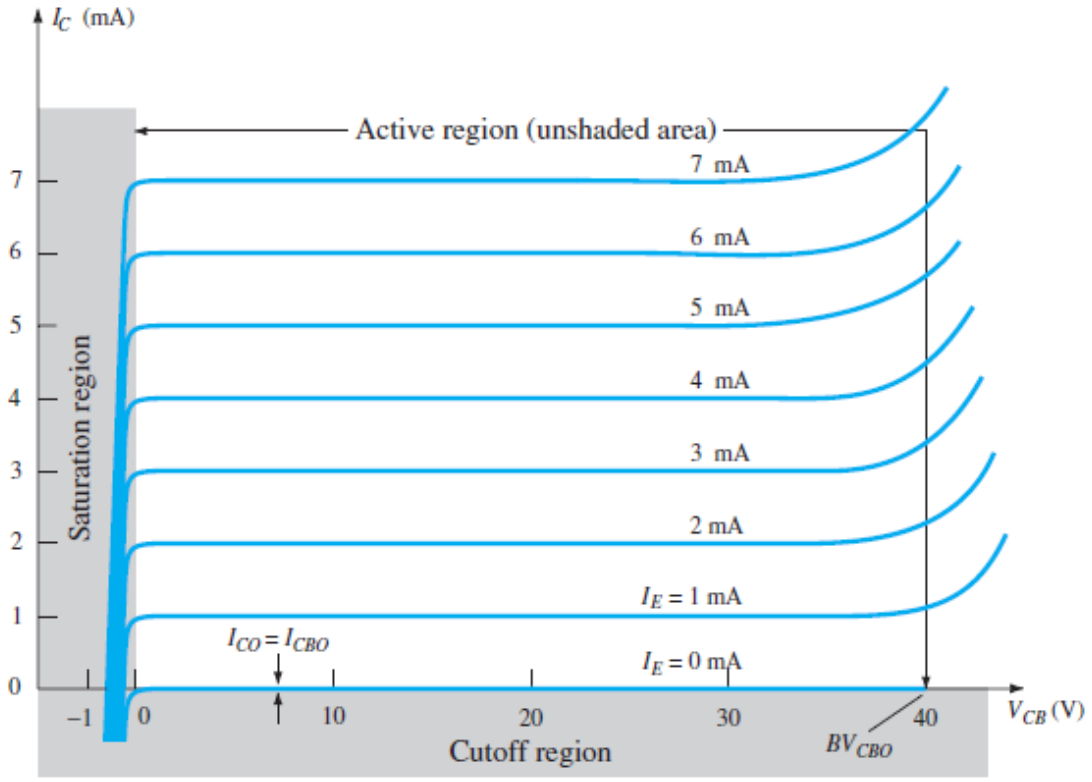


Fig. 9. Output characteristics of common base silicon amplifier.

In particular:

***In the active region the base–emitter junction is forward-biased, whereas the collector base junction is reverse-biased.***

The active region is defined by the biasing arrangements of Fig. 7. At the lower end of the active region the emitter current ($I_E$) is zero, and the collector current is simply that due to the reverse saturation current $I_{CO}$ , as indicated in Fig.10. The current $I_{CO}$ is so small (microamperes) in magnitude compared to the vertical scale of $I_C$ (milliamperes) that it appears on virtually the same horizontal line as $I_C = 0$. The circuit conditions that exist when $I_E = 0$ for the common-base configuration are shown in Fig.10.

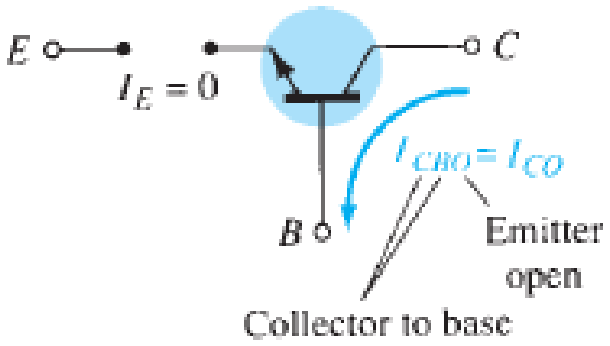


Fig. 10. Reverse saturation current

From the Fig. 9, it is seen that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also the almost negligible effect of $V_{CB}$ on the collector current for the active region. The curves clearly indicate that a first approximation to the relationship between $I_E$ and $I_C$ in the active region is given by

$$I_C \cong I_E$$

As inferred by its name, the cutoff region is defined as that region where the collector current is 0 A, as revealed on Fig. 9 . In addition:

***In the cutoff region the base–emitter and collector–base junctions of a transistor are both reverse-biased.***

The saturation region is defined as that region of the characteristics to the left of $V_{CB} = 0$ V. The horizontal scale in this region was expanded to clearly show the dramatic change in

characteristics in this region. Note the exponential increase in collector current as the voltage $V_{CB}$ increases toward 0 V.

***In the saturation region the base–emitter and collector–base junctions are forward-biased.***

### Alpha (α)

DC Mode In the dc mode the levels of $I_C$ and $I_E$ due to the majority carriers are related by a quantity called alpha and defined by the following equation: where $I_C$ and $I_E$ are the levels of current at the point of operation.

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E + I_{CBO}$$

### COMMON-EMITTER CONFIGURATION

The common emitter configuration is shown in Fig.11. It is called the common-emitter configuration because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals).

### Input Characteristics

The input characteristics of the common-emitter configuration is shown in Fig. 12b. In common base that the input set of characteristics was approximated by a straight-line equivalent that resulted in $V_{BE}$ =0.7 V for any level of $I_E$ greater than 0 mA. For the common-emitter configuration the same approach can be taken,resulting in the approximate equivalent of Fig. 12b. The result supports our earlier conclusion that for a transistor in the “on” or active region the base-to-emitter voltage is 0.7 V. In this case the voltage is fixed for any level of base current.

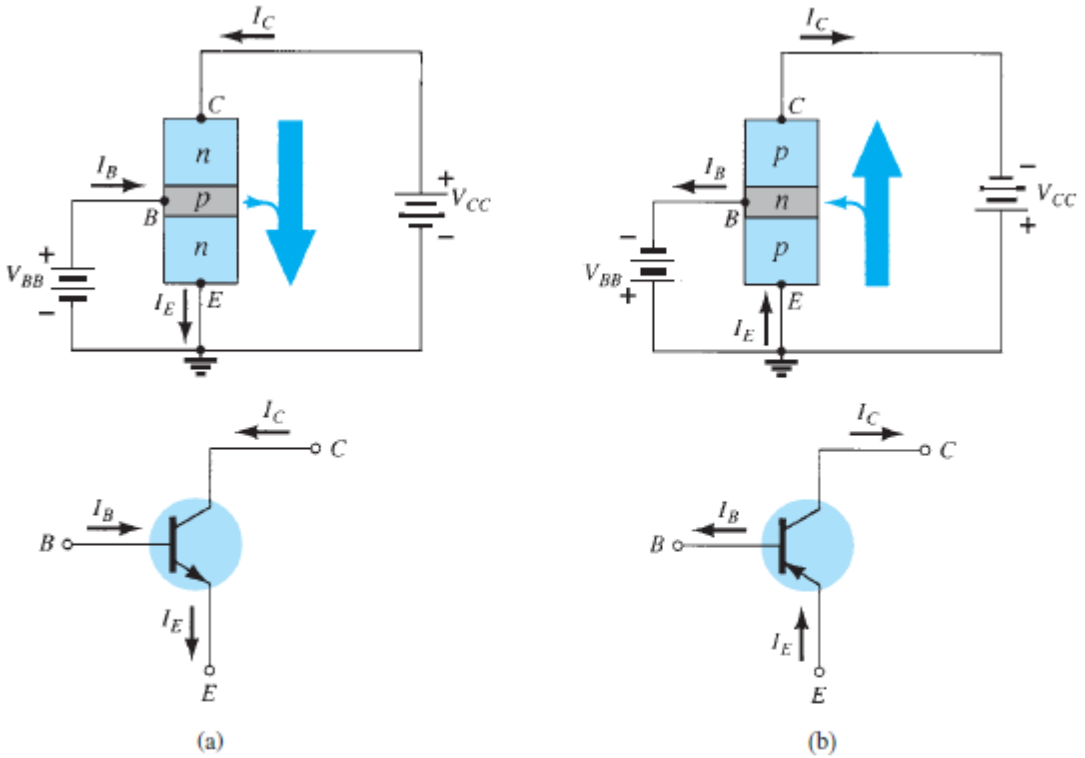


Fig.11. Notation and symbols used with the common-emitter configuration: (a) npn transistor; (b) pnp transistor.

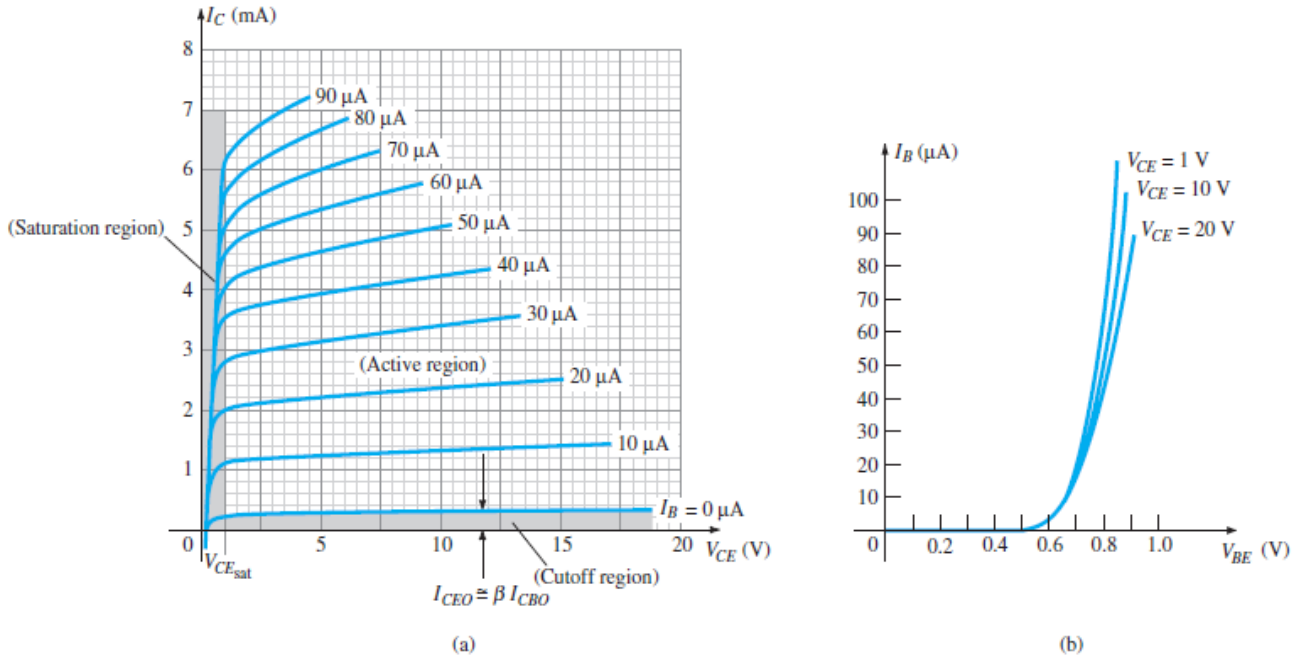


Fig. 12. Characteristics of a silicon transistor in the common-emitter configuration: (a) output characteristics; (b) input characteristics.

**Output Characteristics**

For the common-emitter configuration the output characteristics are a plot of the output current ($I_C$) versus output voltage ($V_{CE}$) for a range of values of input current ($I_B$). The input characteristics are a plot of the input current ($I_B$) versus the input voltage ($V_{BE}$) for a range of values of output voltage ($V_{CE}$). The output characteristics of common-emitter is illustrated in Fig. 12a.

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for $I_B$ are nearly straight and equally spaced. In Fig. 12a this region exists to the right of the vertical dashed line at $V_{CE\,sat}$ and above the curve for $I_B$ equal to zero. The region to the left of $V_{CE\,sat}$ is called the saturation region.

***In the active region of a common-emitter amplifier, the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.***

The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig.12a that $I_C$ is not equal to zero when $I_B$ is zero. A small current exist even if the $I_B = 0$ as illustarated in Fig.13. For the common-base configuration, when the input current $I_E$ was equal to zero, the collector current was equal only to the reverse saturation current $I_{CO}$ , so that the curve $I_E$ =0 and the voltage axis were, for all practical purposes, one.

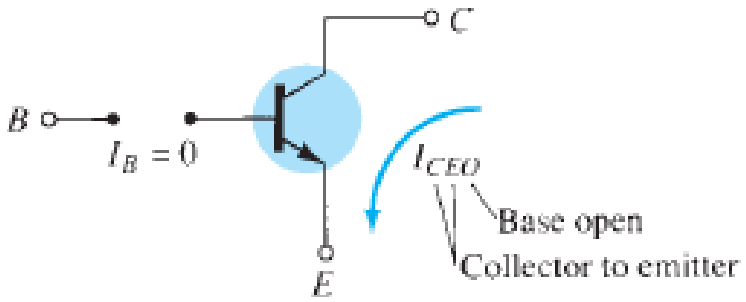


Fig.13 Circuit condition related to $I_{CEO}$.

From the common base characteristics

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

If we consider the case discussed above, where $I_B = 0$ A, and substitute a typical value of a such as 0.996, the resulting collector current is the following:

$$I_C = \frac{\alpha(0\text{ A})}{1-\alpha} + \frac{I_{CBO}}{1-0.996}$$
$$= \frac{I_{CBO}}{0.004} = 250 I_{CBO}$$

If $I_{CBO}$ were 1 mA, the resulting collector current with $I_B = 0$ A would be 250(1 mA) = 0.25 mA, as reflected in the characteristics of Fig.12a.

The collector current defined by the condition $I_B = 0$ mA can be expressed as

$$I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\,\mu A}$$

A relationship can be developed between $\beta$ and $\alpha$ using the basic relationships introduced thus far. Using $\beta = I_C/I_B$, we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$
$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

*and dividing both sides of the equation by* $I_C$ results in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{\beta + 1}}$$

or

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}}$$

In addition, recall that

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

but using an equivalence of

$$\frac{1}{1 - \alpha} = \beta + 1$$

derived from the above, we find that

$$I_{CEO} = (\beta + 1)I_{CBO}$$

or

$$\boxed{I_{CEO} \cong \beta I_{CBO}}$$

$$\boxed{I_C = \beta I_B}$$

$$I_E = I_C + I_B$$
$$= \beta I_B + I_B$$

$$\boxed{I_E = (\beta + 1)I_B}$$

`

## Equations

$$I_E = I_C + I_B, \qquad I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}, \qquad V_{BE} \cong 0.7\ \text{V}$$

$$\alpha_{\text{dc}} = \frac{I_C}{I_E}, \qquad \alpha_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}, \qquad I_{CEO} = \left.\frac{I_{CBO}}{1 - \alpha}\right|_{I_B = 0\,\mu\text{A}}$$

$$\beta_{\text{dc}} = \frac{I_C}{I_B}, \qquad \beta_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}, \qquad \alpha = \frac{\beta}{\beta + 1}$$

$$I_C = \beta I_B, \qquad I_E = (\beta + 1)I_B, \qquad P_{C_{\text{max}}} = V_{CE}I_C$$