

## Biasing of Transistor

→ Faithful amplification :- when the weak signal is amplified using transistor, it is ensure that the output signal shape must be resembles to the input signal shape. This amplification of the signal without the change in its shape is known as faithful amplification.

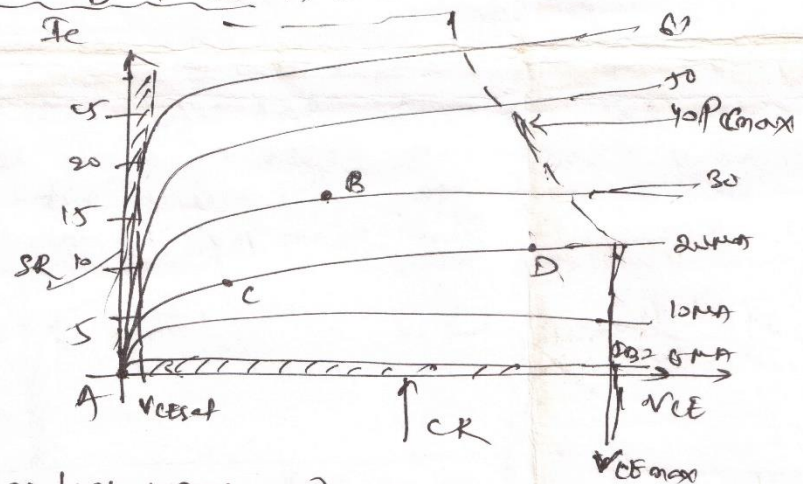
→ To achieve faithful amplification we have to let the Q point ~~in such a way that we get~~ <sup>by using some means</sup> ~~using~~ proper connection, that is called biasing. usually Q point set in the middle of the dc load line.

Defn The proper flow of zero signal collector current & the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing.

### Necessity of biasing :-

To get faithful amplification, we need proper biasing ckt. If the transistor is not biased properly, it would work inefficiently & produce distortion in the output signal.

### operating point :-



→ If no bias were used, the device would initially be ~~with~~ completely off, resulting in a Q point at A - namely zero current through the device. ~~But~~ It is necessary to bias a device so that it can respond to the entire range of the output signal, point A would not be suitable.

→ For point B, if a signal is applied to the ckt, the device will vary in current & voltage from the operating point, allowing the device to react to both ~~++~~



②  $V_{CE} = 0V$  &  $I_C = 0mA$ . Operating point C also raises some concern about the nonlinearity introduced by the fact that the operating beta  $\beta_B$  curve is rapidly changing in this region.

In general it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of the input signal is same. Point B is in a region of more linear swing & therefore more linear operation.

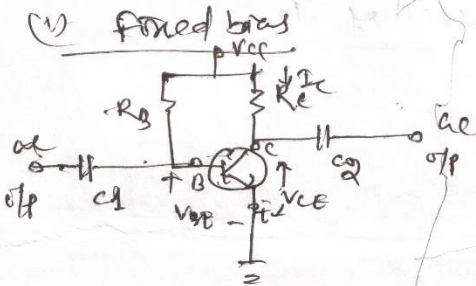
Point D sets the device operating point near the max. voltage & power level. One off voltage swing is limited if the max. voltage is not to be exceeded.

Point B therefore seems the best operating point in terms of linear gain & largest possible voltage & current swing.

Different types of biasing ckt ↓

(3)

- (i) fixed bias
- (ii) self/biased or auto-biased bias
- (iii) voltage divider bias
- (iv) DC collector feedback bias.



$$X_{ie} = \frac{1}{2m\beta} = \frac{1}{\beta} \approx \frac{1}{100}$$

Q/P mode

$$V_{CC} - I_B R_B - V_{BE} = 0V$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$V_{CC}, R_B, V_{BE}$  are constant, so  $I_B$  is constant.

Q/P mode

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C \quad \& \quad I_C \approx \beta I_B$$

$$V_{CE} = V_{CC} - \beta I_B R_C \quad \text{Here } V_{CE} = 20V$$

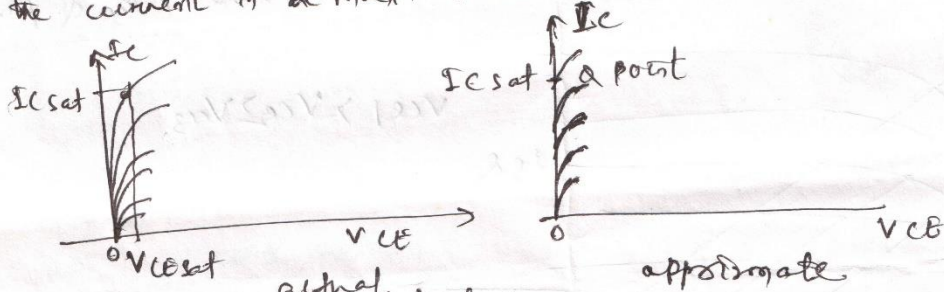
$$V_{CE} = V_{CC}$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B \quad (\because V_E = 0V)$$

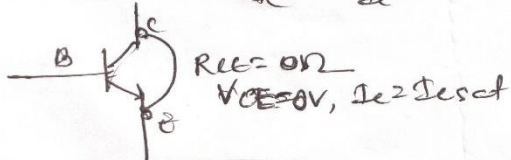
Transistor Saturation

The term saturation is applied to any system where levels have reached their max<sup>m</sup> value.  
 For a transistor operating in the saturation region, the current is a max<sup>m</sup> value for the particular design.



the current is <sup>actual</sup> <sup>relatively</sup> high & the VCE is assumed to be 0V.

So  $R_{E8} \approx \frac{V_{CE}}{I_C} = \frac{0V}{I_C} = 0\Omega$  s.e.

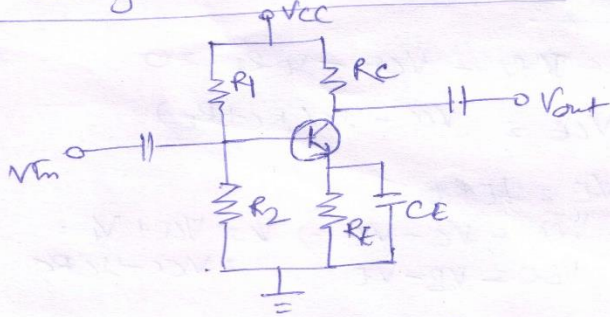


$$I_{Csat} = \frac{V_{CE}}{R_E}$$

$V_{CE} = 20V$

... by the <sup>initial</sup> potentials of

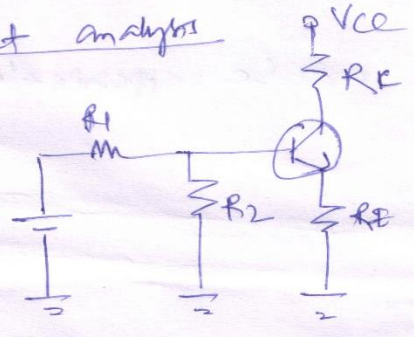
2. Voltage divider bias ckt.



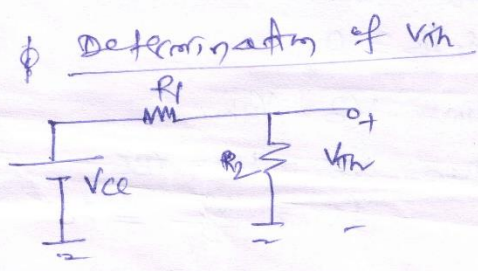
- (1) Exact analysis
- (2) Approximate analysis.

Why voltage divider bias is named?  
 As the input side fed with ~~the supply dc voltage~~ the supply dc voltage <sup>which</sup> divided using two resistors  $R_1$  &  $R_2$ , ~~therefore~~ <sup>is</sup> so called as voltage divider bias ckt.

1) Exact analysis

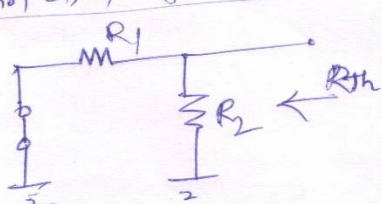


Applying Thevenin theorem find the single voltage  $V_{th}$  & resistance  $R_{th}$



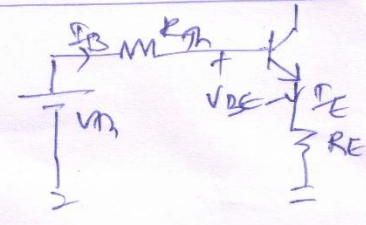
$$V_{th} = \frac{R_2 \times V_{CC}}{R_1 + R_2}$$

Determination of  $R_{th}$



$$R_{th} = R_1 \parallel R_2$$

Apply KVL at input loop



$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

$$I_C \approx I_E = (\beta + 1) I_B$$

Applying KVL to the output loop, we get

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

**Approximate Analysis:**

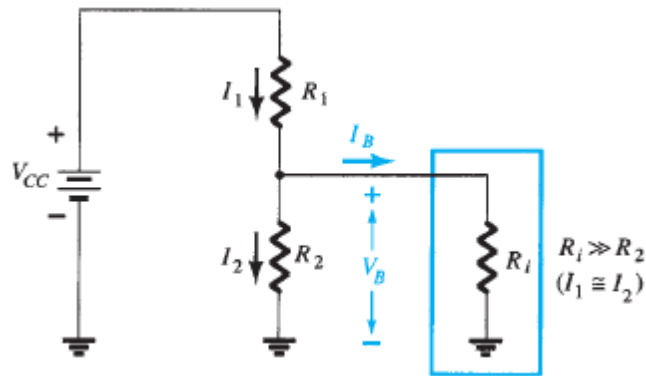


Fig. Partial bias circuit for calculating the approximate base voltage  $V_B$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$R_i = (\beta + 1)R_E \cong \beta R_E$$

The condition for approximation is

$$\beta R_E \geq 10R_2$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

$$I_{CQ} \cong I_E$$

The collector to emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

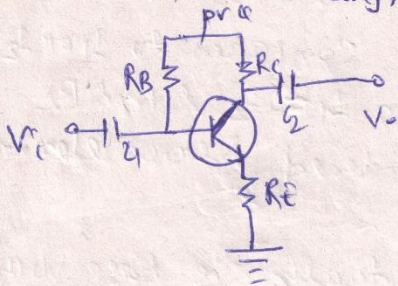
but because  $I_E \cong I_C$ ,

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

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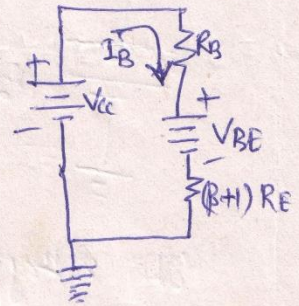
←: Emitter Bias Configuration →

→ Emitter resistor to improve the stability level over that of fixed bias configuration.

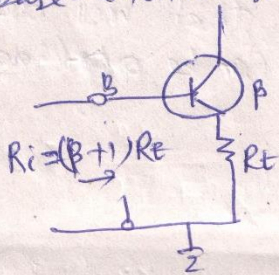


QIP Loop

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$



NOTE :- Aside from the base-emitter voltage  $V_{BE}$ , the resistor  $R_E$  is reflected back to the i/p by a factor  $(\beta + 1)$ . In other words, the emitter resistor which is part of the collector-emitter loop "appears as"  $(\beta + 1)R_E$  in the base-emitter loop. But  $\beta$  is typically 50 or more, the emitter resistor appears to be a great deal larger in the base ckt.



$$R_i = (\beta + 1)R_E$$

o/p loop

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$\& V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_B = V_{CC} - I_B R_B$$

$$V_C = V_{CE} + V_E$$

$$V_B = V_{BE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$