MACHINE LANGUAGE INSTRUCTION FORMATS:

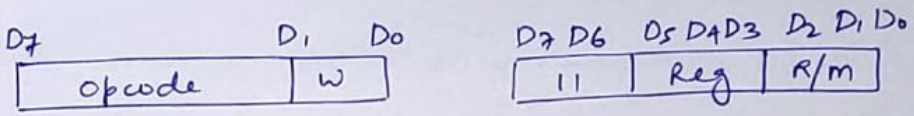
* Instruction - opcode + operands.
* 6 - types of instruction formats:-

(a) One byte instruction

- one byte long
- has emplied data or register operands.
- LSB 3-bits are used to specify register (if any) else, all 8-bit opcode and operands are emplied.

(b) Register to Register:

- 2 bytes long.

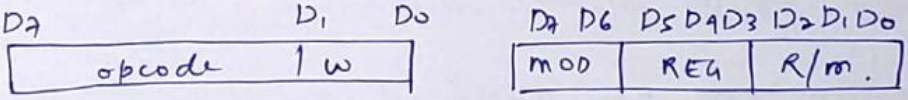


W = width of operand.

R/m = Register or memory location,

(c) Register to/from memory with no displacement:

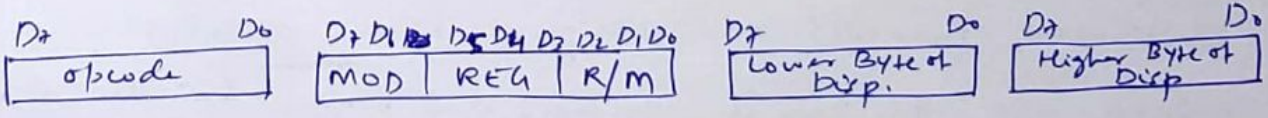
- 2 bytes long



MOD = mode of addressing

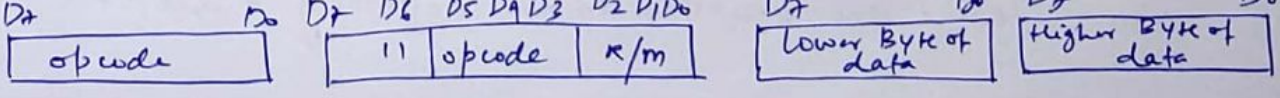
(d) Register to/from memory with displacement:

- 2 bytes as previous + extra 1 or 2 bytes for displacement.



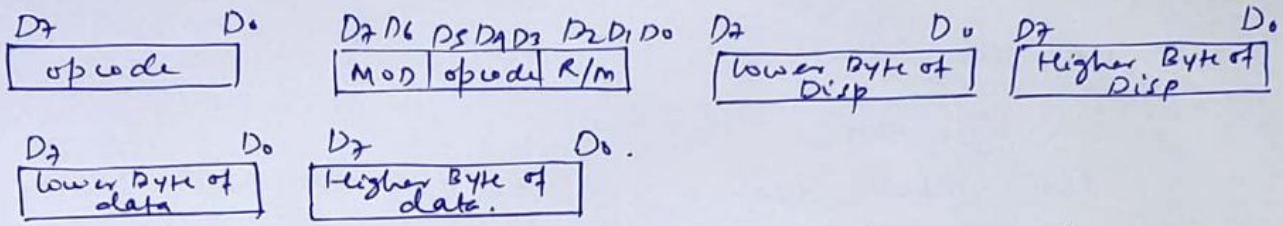
(e) Immediate operand to Register:

* 3 - additional bits for opcode in REG field of register to register type.



f) Immediate operand to memory with 16-bit displacement:

* 5 or 6 bytes long.



single bit indicators of opcodes

W = 0 (8-bit operand)
= 1 (16-bit operand)

D = 0 (REG is source)
= 1 (REG is destination).

S = 0 W = 0 (8-bit operation with 8-bit immediate operand)

S = 0 W = 1 (16-bit operation with 16-bit immediate operand)

S = 1 W = 1 (16-bit operation with sign extended immediate data).

V = 0 (Shift count is 1)
= 1 (if CL register contains shift count)

Z = 1 (instruction with REP prefix is executed)
= 0 (repeating instruction stops)
↳ matched with zero flag of Flag Register.

* The register code of different registers (either as source or destination operands) are assigned binary codes.

* There are 4-segment registers ⇒ 2 binary bits are sufficient to encode them

* The other registers are 8 in number. To code their 8-bit and 16-bit variants, they are combined with the w-bit. The details are presented on the following table :-

Code Assignment to different Registers:-

W	Register code	Registers
0	000	AL
0	001	CL
0	010	DL
0	011	BL
0	100	AH
0	101	CH
0	110	DH
0	111	BH
1	000	AX
1	001	CX
1	010	DX
1	011	BX
1	100	SP
1	101	BP
1	110	SI
1	111	DI

segment (2 bit Register code)	Register
00	ES
01	CS
10	SS
11	DS

NOTE:-

* All addressing modes have DS as default data segment.
* Addressing modes using BP and SP have SS as the default segment register.
* MOD and R/m fields of a particular instruction can be decided from the addressing mode of the instruction.

→ The addressing modes and corresponding MOD, REG and R/m fields can be obtained from the following table:-

..P.T.O.

Operands / MOD / R/M	Memory operands: No displacement 00	Memory operands: Displacement (8-bit) 01	Memory operands: Displacement (16-bit) 10	Register operands: 11 W=0	Register operands: 11 W=1
000	(BX)+(SI)	(BX)+(SI)+D8	(BX)+(SI)+D16	AL	AX
001	(BX)+(DI)	(BX)+(DI)+D8	(BX)+(DI)+D16	CL	CX
010	(BP)+(SI)	(BP)+(SI)+D8	(BP)+(SI)+D16	DL	DX
011	(BP)+(DI)	(BP)+(DI)+D8	(BP)+(DI)+D16	BL	BX
100	(SI)	(SI)+D8	(SI)+D16	AH	SP
101	(DI)	(DI)+D8	(DI)+D16	CH	BP
110	D16	(BP)+D8	(BP)+D16	DH	SI
111	(BX)	(BX)+D8	(BX)+D16	BH	DI

NOTE :-

* D8 - 8 bit displacement
  D16 - 16 bit displacement.
* Default segment while using BP and SP is SS.
  for all others, it is DS or ES,

ADDRESSING MODES OF 8086 :-

* It indicates a way of locating data/operands.
* An instruction may belong to one/more addressing modes depending on the type of operands and the way they are accessed for executing an instruction.

Types of Instructions:

1. Sequential control flow instructions.
2. Control Transfer instructions

⇒ Different addressing modes are as follows:-

1. Immediate:-

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MOV AX, 0005H
MOV BL, 06H   = Immediate data.
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(2) Direct:-

MOV AX, [5000H] → data on location 5000H is transferred to register AX.

segment address = content of DS

offset " = 5000H.

Effective address = 10H * DS + 5000H

IN 80H → 80H is I/O address

(3) Register:-

MOV BX, AX
ADC AL, BL } all operands in registers.

(4) Register Indirect:-

MOV AX, [BX] BX contains offset address
or
SI Segment address = content of DS or ES
or
DI Effective address = 10H * DS + [BX]

(5) Indexed:-

* offset is stored in index registers.
* default segment register = DS
* In string instruction - default segment register = DS or ES.
* special case of indirect addressing mode.

MOV AX, [SI] → Effective address = 10H * DS + [SI]
MOV CX, [DI]

(6) Register Relative:-

* 8-bit/16-bit displacement added to any one of the registers among BX, BP, SI and DI in DS or ES segment.

MOV AX, 50H [BX] → Effective address = 10H * DS + 50H + [BX]

Displacement = 50H

MOV 10H[SI], DX

⑦ Based Indexed:-

* Effective address is formed by adding content of base register (BX or BP) to the content of an index register (SI/DI).
* Default segment register = DS or ES.

MOV AX, [BX][SI] — Effective address (EA) = 10H + DS + [BX] + [SI]

Base, Index

content at EA is moved to register AX.

MOV [BX][DI], AX

⑧ Relative Based Indexed:-

* same as previous case with an extra immediate 8-bit or 16-bit displacement.

MOV AX, 50H [BX][SI] ⟶ Effective address = 10H + DS + [BX] + [SI] + 50H

ADD 50H [BX][SI], BP

→ For control transfer instructions, addressing mode depends on whether the destination location is within the same or different segment

* It also depends on method of passing the destination address to the processor.

Modes for Control Transfer Instructions

- Intersegment
  - Direct
  - Indirect
- Intrasegment
  - Direct
  - Indirect.

(9) Intrasegment Direct Mode :-

* address appears on the instruction as immediate displacement value.
* displacement is computed relative to content of IP.
* short jump - signed displacement (d) is of 8-bits. ($-128 < d < +127$)
* long jump - signed displacement (d) is of 16-bits ($-32768 < d < +32767$)

JMP SHORT LABEL — Label lies within (−128) to (+127) from current IP content.

(10) Intrasegment Indirect :-

JMP [Bx] → Jump to effective address = 10H * IP + [Bx]

(11) Intersegment Direct :-

JMP 5000H : 2000H (5000H → code segment, 2000H → IP)

Effective address = 10H * CS + IP
= 10H * 5000H + 2000H
= 50000H + 2000H
= 52000H

(12) Intersegment Indirect :-

JMP [2000H] — Value at [2000H] location in DS is the displacement of the location in the other segment. (Let this value is x)

Effective address = 10H * CS + IP + x

Q Given the contents of different registers, form the Effective addresses for different addressing modes under sequential instructions category :

offset (displacement) = 5000 H

[AX] = 1000H, [BX] = 2000H, [SI] = 3000 H, [DI] = 4000 H,

[BP] = 5000 H, [SP] = 6000H, [CS] = 0000 H, [DS] = 1000 H,

[SS] = 2000 H, [IP] = 7000 H

1. MOV AX, [5000H]
2. MOV AX, [BX]
3. MOV AX, 5000[BX]
4. MOV AX, [BX][SI]
5. MOV AX, 5000 [BX][SI]

Find the type of addressing mode in each case and also calculate the effective address.

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Reference :-
Advanced Microprocessors and Peripherals
(K.M. Bhurchandi & A.K. Ray)
McGraw Hill Education,