# Module - II (JFET, MOSFET, CMOS)



A field-effect transistor (FET) is a three terminal (namely drain, source and gate) semiconductor device in which current conduction is by only one type of majority carriers.

There are two major categories of FET

(i) Junction field-effect transistor (JFET)

(ii) Metal-oxide-semiconductor field effect transistor (MOSFET)

## Difference between BJT and FET

| BJT | FET |
|---|---|
| 1) BJT transistor is a current-controlled device. The output current $I_C$ is a direct function of the level of $I_B$. | 1) The JFET transistor is voltage-controlled device. The FET current I is the function of the voltage $V_{GS}$ applied to the input circuit. |
| 2) It is a bipolar device - the prefix bi means that the conduction level is a function of two charge carriers, electrons and holes. | 2) The FET is a unipolar device, i.e depending solely on either electrons or holes conduction. |
| 3) Low input impendance | 3) High input impendance. |
| 4) Less temperature stable. | 4) FETs are more temperature stable than BJT. |
| 5) BJTs are usually larger in construction than FET. | 5) FETs are usually smaller in construction than BJT. |

## Junction Field Effect Transistor (JFETs)

JFETs are of two types
- N-channel JFETs
- P-channel JFETs

**Basic construction :-**

In an N-channel JFET an N type Silicon bar is referred to as the channel. It has two smaller pieces of P-type silicon material diffused on the opposite

sides of its middle part forming the P-N junction.

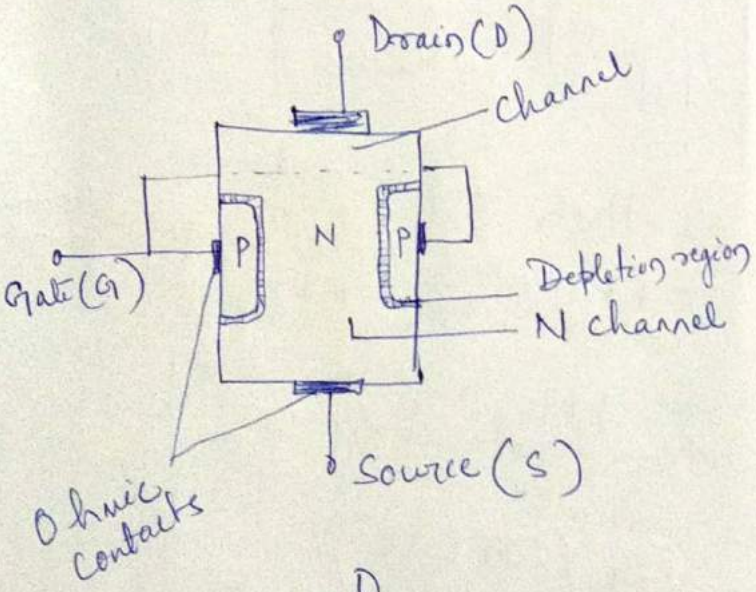
The three terminals are

(i) Source :- The terminal through which the majority carriers enter the channel is called the source terminal S and the conventional current entering the channel at S is denoted as $I_S$.

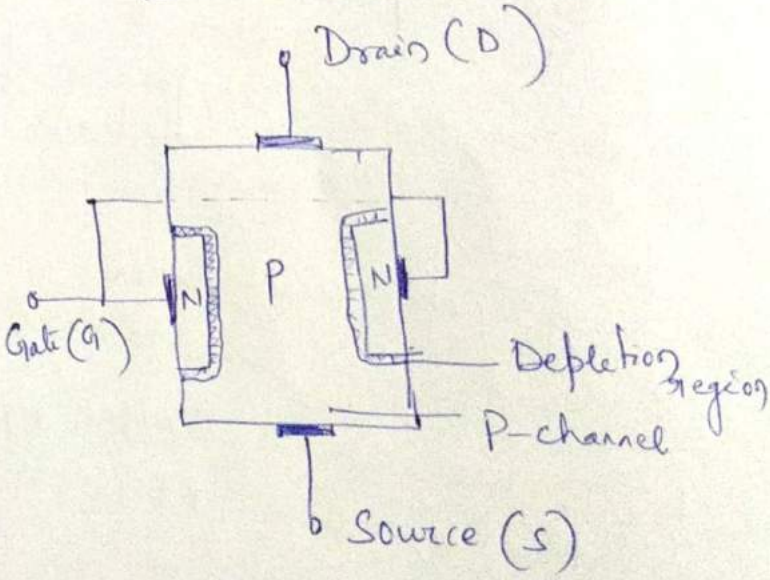
(ii) Drain :- The terminal through which the majority carriers leave the channel is known as drain terminal D and the conventional current leaving the channel D is designated as $I_D$.

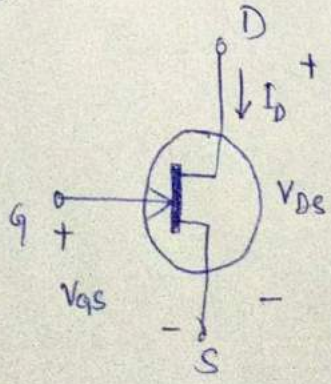
(iii) Gate :- There are two externally connected heavily doped impurity regions ~~formed by alloying by~~ to create two P-N junctions. These impurity regions are called the gate G. A voltage $V_{GS}$ is applied between the gate and source in the direction to reverse bias the P-N junction.

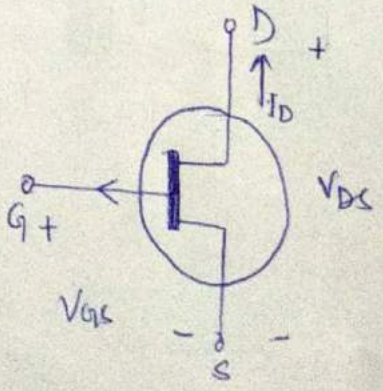
N-channel JFET




P-channel JFET



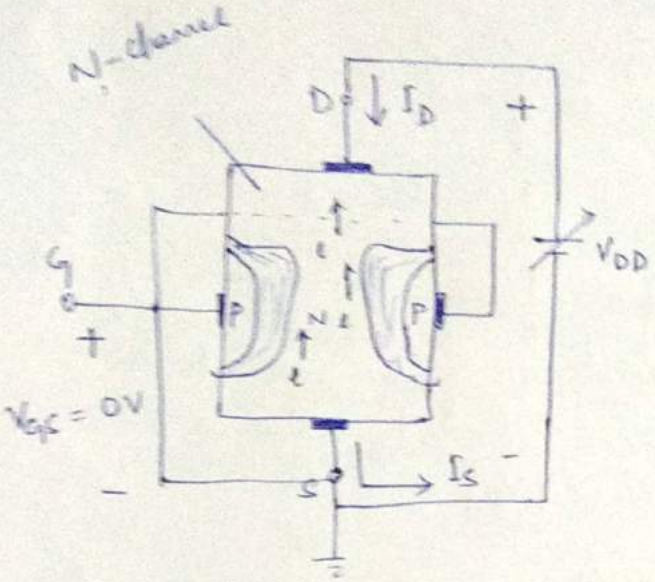



## N-channel device (majority charge carriers are electrons)

Case-1

i) $V_{GS} = 0V$, $V_{DS} > 0V$ (No bias condition)

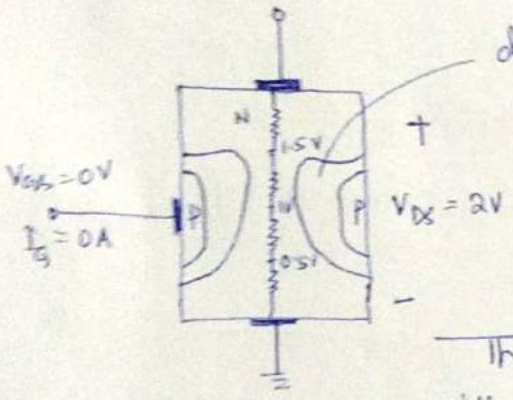



A positive voltage $V_{DS}$ is applied across the channel and gate is connected to the source to make $V_{GS} = 0V$.

It is no-bias condition.

When $V_{DS}$ is applied, the electrons will be drawn towards the drain.

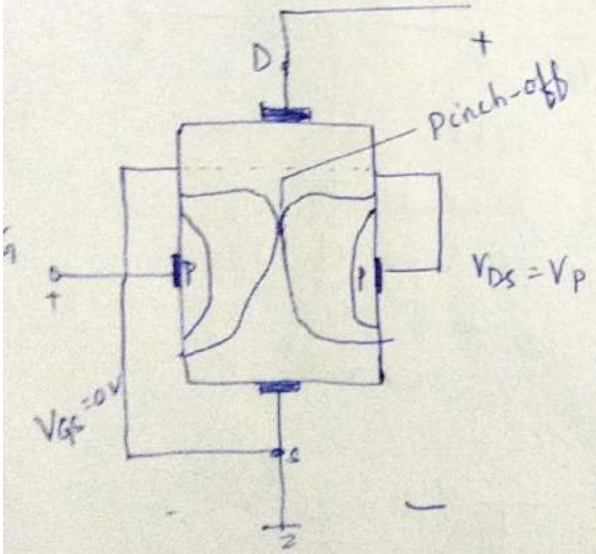
Hence $\boxed{I_D = I_S}$, $\boxed{I_G = 0\,A}$




This is because

→ Assuming a uniform resistance in the n-channel, the resistance of the channel can be broken down to the dimensions.

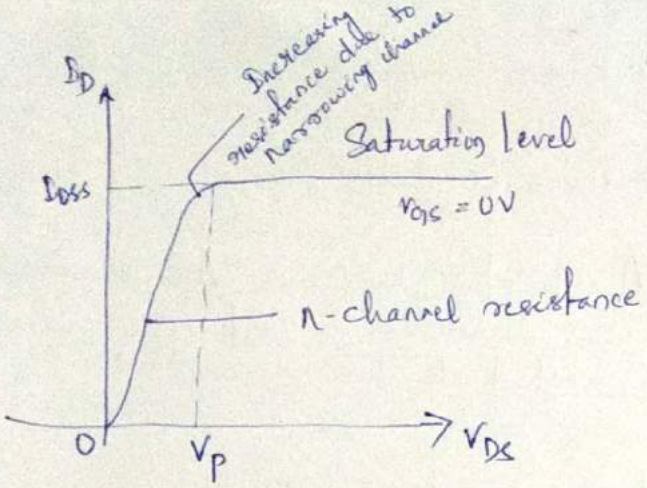
Therefore, the upper region of the p-type material will be reverse-biased by about 1.5V with lower region reverse-biased by 0.5V.




As $V_{DS}$ increases further it approaches a level $V_P$, resistance increases resulting reduced path conduction.

If $V_{DS}$ is increased to a level ~~where it~~ where the two depletion regions touches each other, the condition is called <u>pinch-off</u>.

The level of $V_{DS}$ that establishes this condition is referred to as <u>pinch-off voltage</u>; which is denoted by <u>$V_P$</u>.




( $I_D$ vs $V_{DS}$ for $V_{GS} = 0V$)

At pinch ~~voltage~~ off voltage $I_D$ maintains a saturation level $I_{DSS}$.

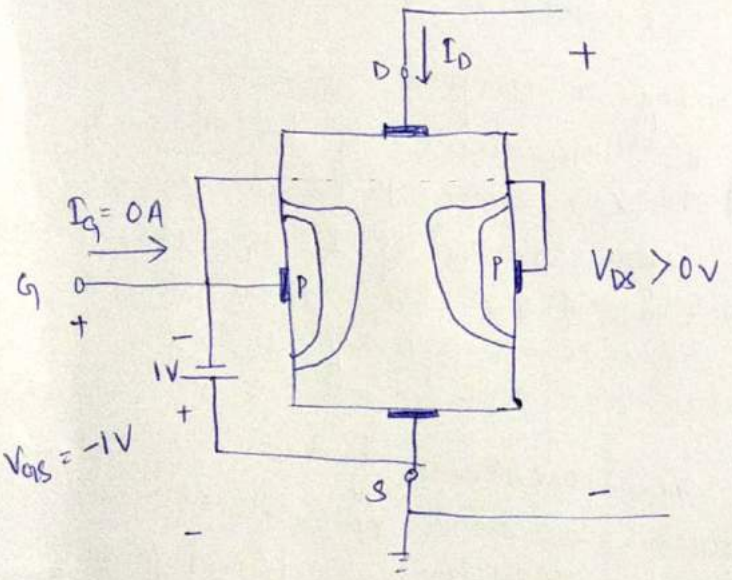
When $V_{DS} > V_P$, the current is fixed.

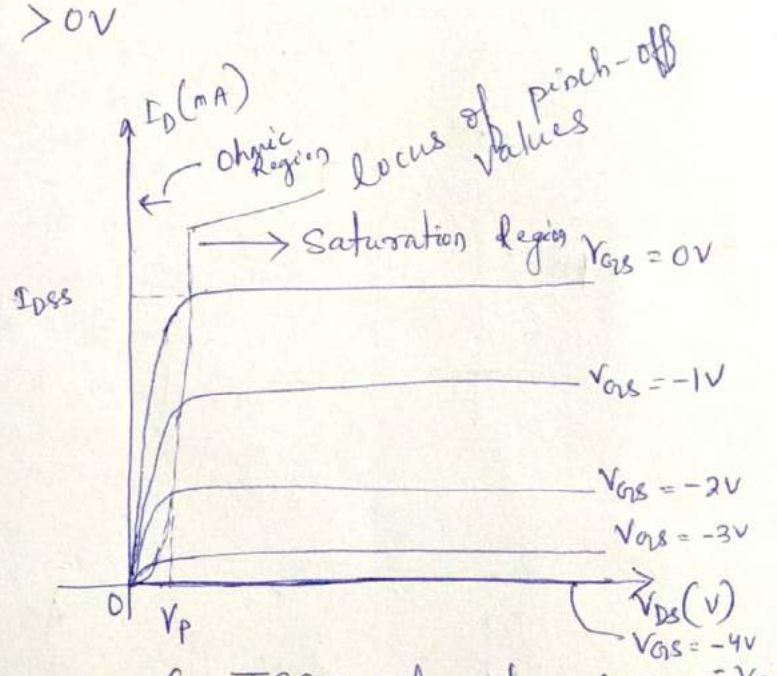
$$\boxed{I_D = I_{DSS}}$$

$I_{DSS}$ = Drain-to-Source current with a short-circuit connection from gate to source.

$I_{DSS}$ is the ~~max~~ maximum drain current ~~when~~ in the conditions $V_{GS} = 0V$ and $V_{DS} > |V_P|$.

ii) <u>Case-II</u> :- $V_{GS} < 0V$, $V_{DS} > 0V$




( JFET characteristic)

— The result of applying a negative bias to the gate to reach the saturation level at a lower level of $V_{DS}$.

— The resulting saturation level for $I_D$ has been reduced and will continue to decrease as $V_{GS}$ is made more and more negative.

When $\boxed{V_{GS} = -V_P, \ I_D = 0mA}$ The device is turned off.

## Voltage-Controlled Resistor

→ The region to the left of the pinch-off locus is referred to as the ohmic or voltage-controlled resistance region.

→ In this region, the JFET can be employed as a variable resistor whose resistance is controlled by the applied gate-to-source voltage.

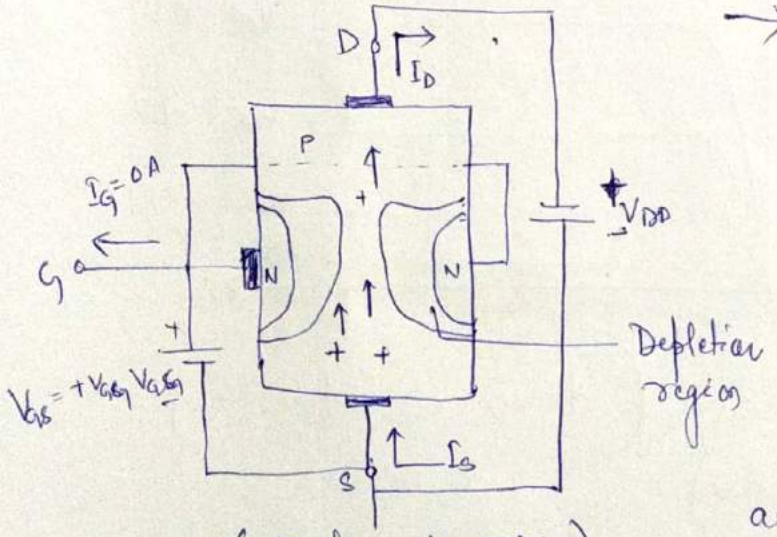
→ When $V_{DS} < V_P$, the resistance of the channel is a function of the applied voltage $V_{GS}$.

If $r_0$ is the resistance with $V_{GS} = 0V$,
$r_d$ = resistance at a particular level of $V_{GS}$.

Then $r_d$ in terms of the applied voltage $V_{GS}$ is

$$r_d = \frac{r_0}{\left(1 - V_{GS}/V_P\right)^2}$$

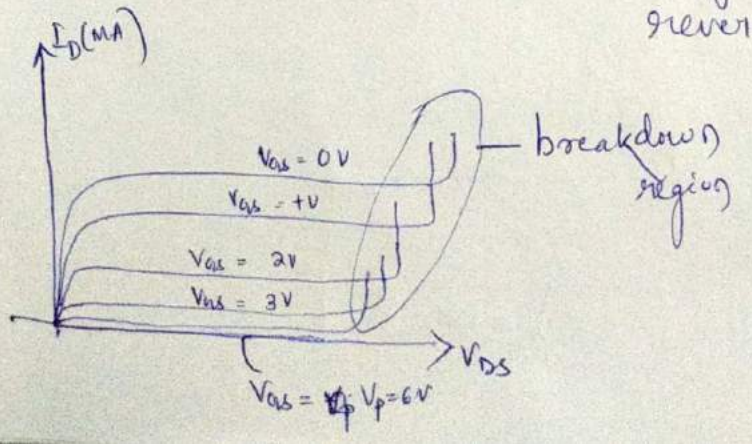
## P-channel JFET




(P-channel JFET)

→ The p-channel JFET is constructed in exactly the same manner as the N-channel device with a reversal of the p and N type materials.

→ The current directions are reversed and the actual polarities for the voltages $V_{GS}$ and $V_{DS}$ are reversed.



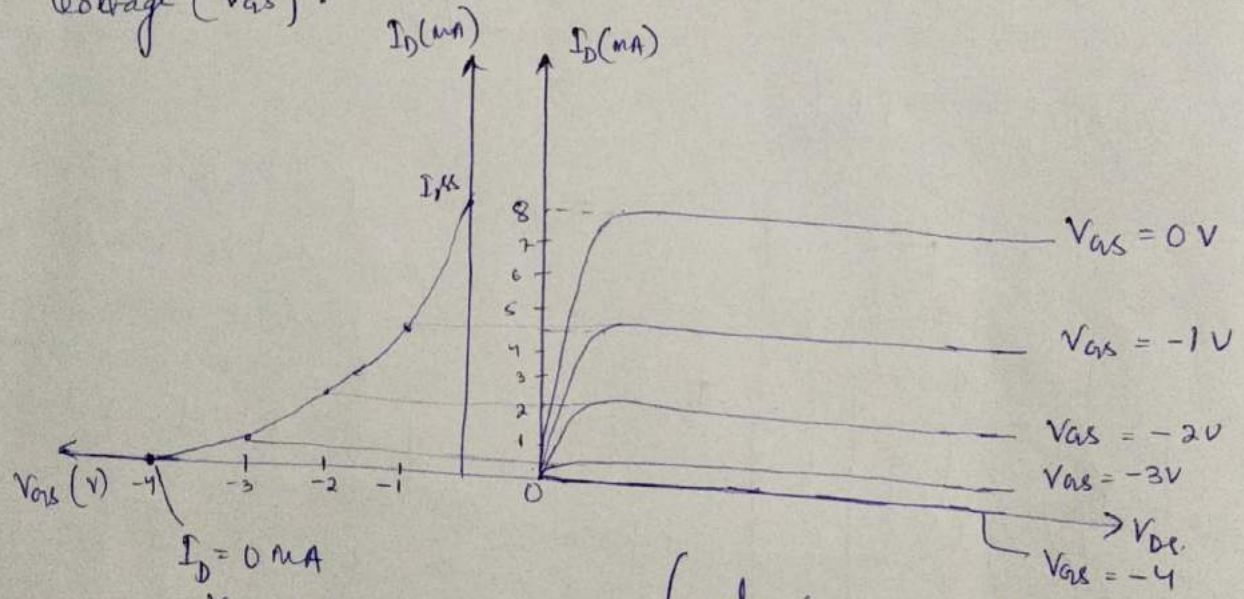
# Transfer characteristics

The relationship between $I_D$ and $V_{GS}$ is defined by Shockley's equation.

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

The transfer characteristics are a plot of an output or drain current versus an input-controlling quantity i.e voltage.

→ Hence transfer characteristic can be determined experimentally, Keeping drain source voltage ($V_{DS}$) constant and determining drain current ($I_D$) for various values of gate-source voltage ($V_{GS}$).




(Transfer characteristic)

(drain characteristic)

(Obtaining the transfer curve from the drain characteristic)

from the Schockley's Equation

$$\boxed{V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)}$$

# Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs)

MOSFET is an important semiconductor device and is widely employed in many circuit applications.

MOSFET are of two types

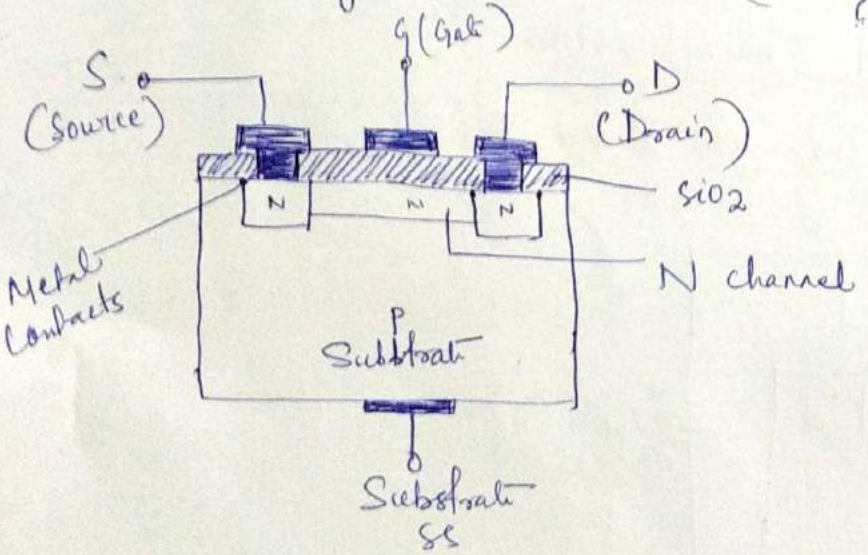
(i) Depletion-type MOSFET (De-MOSFET)

(ii) Enhancement-type MOSFET (E-MOSFET

~~Deption~~ Depletion-type MOSFET :- Here, a channel is physically constructed and a current between drain and source is due to voltage applied across the drain-source terminals.

Enhancement-type MOSFET :- It has no channel ~~between~~ formed during the construction between drain and source. Voltage is applied to the gate to develop a channel of charge carriers so that a current results when a voltage is applied across the drain-source terminals.

## Depletion-Type MOSFET (N-channel Depletion Type MOSFET)




(N-channel depletion type MOSFET)

→ The substrate is the foundation upon which the device is constructed and is formed from a slab of P-type material.

→ The substrate is internally connected to the source terminal.

→ The source and drain terminals are connected through N-channel.

→ The gate is connected to a metal contact surface but remains insulated from the N-channel by a very thin $SiO_2$ layer.

→ $SiO_2$ is an ~~insulator~~ insulating material / dielectric, so that there is no direct electrical connection between the gate terminal and the channel of the MOSFET.

Due to this insulating layer of $SiO_2$, MOSFET offers very high input impendance.

Hence, the name

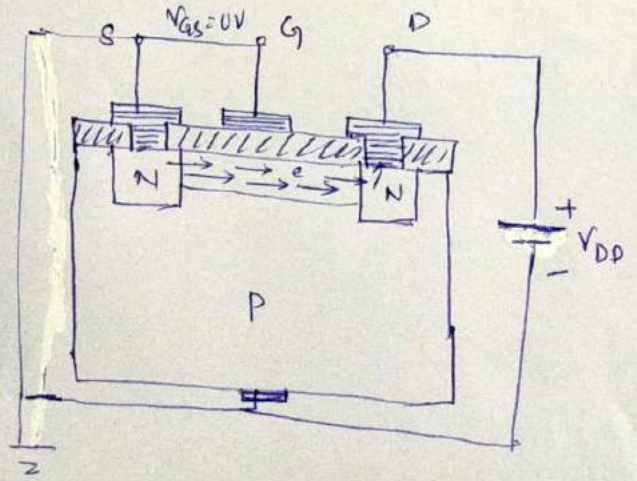
MOSFET — Field effect transistor

- M — Metal (drain, source and gate connections to the proper surface)
- O — Oxide (silicon dioxide $SiO_2$ insulating layer)
- S — Semiconductor (basic structure on which p and N type regions are deffused)

★ MOSFET is also known as insulated - gate FET or IGFET.

## Basic operation and characteristics

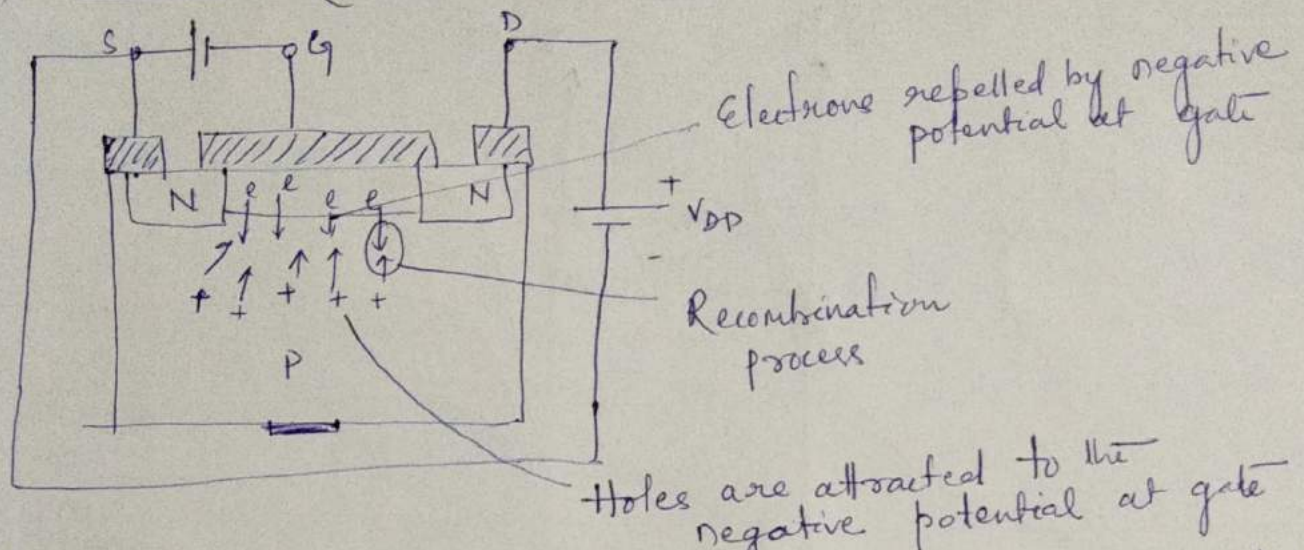
i) Case - I ($V_{GS} = 0V$, $V_{DS} > 0V$)




($V_{GS} = 0V$ and an applied voltage $V_{DD}$)

→ When $V_{DS}$ is applied, the positive potential at the drain attracts free electrons of the N-channel, and the current $\boxed{I_D = I_{DSS}}$

(ii) Case - II ( $V_{GS} < 0V$, $V_{DS} > 0V$ )




→ The negative potential at the gate pressures electrons towards the p-type and attracts holes from the p-type substrate.

→ As the magnitude of negative bias increases, the level of recombination between electrons and holes increases resulting decrease in the number of free electrons available for conduction.

→ Therefore, drain current decreases with increasing negative bias for $V_{GS}$.

→ When $V_{GS} = -V_P$, $I_D = 0$ ( $V_P$ = pinch-off voltage )

(iii) Case - III ( $V_{GS} > 0V$, $V_{DS} > 0V$ )

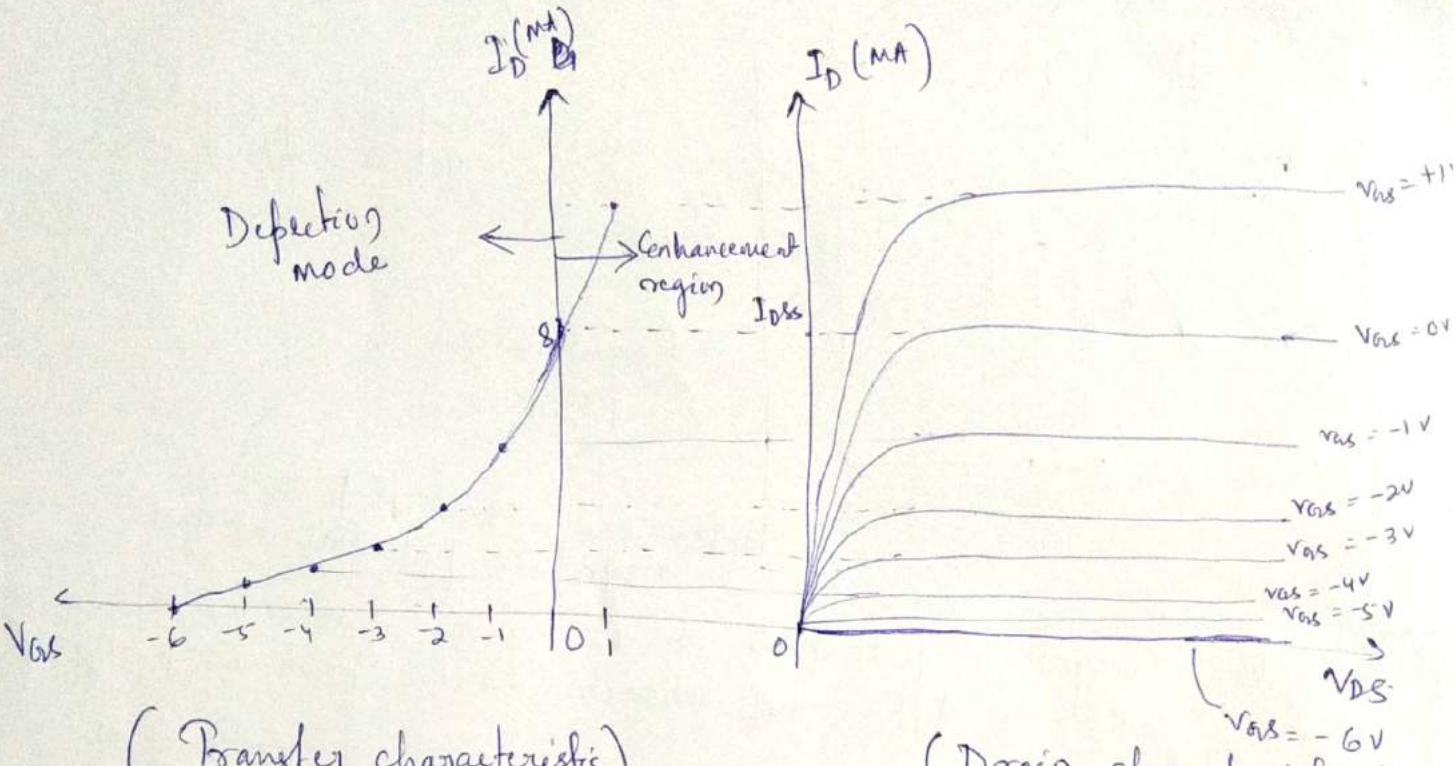
→ The positive values of $V_{GS}$ or the positive potential at the gate terminal attracts free electrons from the p-substrate.

→ Hence, the increase in $V_{GS}$ in the positive direction, ~~set~~ reveals that the drain current increases at a rapid rate.

→ The application of a positive $V_{GS}$ enhanced the level of free carriers in the channel.

~~Relationship~~ Relation between $I_D$ and $V_{GS}$ is given by

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$




(Transfer characteristic) (Drain characteristic)

→ The region of positive gate voltage on the drain ~~&~~ or transfer characteristic is referred to as the <u>enhancement region</u>.

→ The region between cut-off and the saturation level of $I_{DSS}$ is referred to as the <u>depletion region</u>.

★ The transfer characteristic curve in depletion type MOSFET is defined by Shockley's equation.