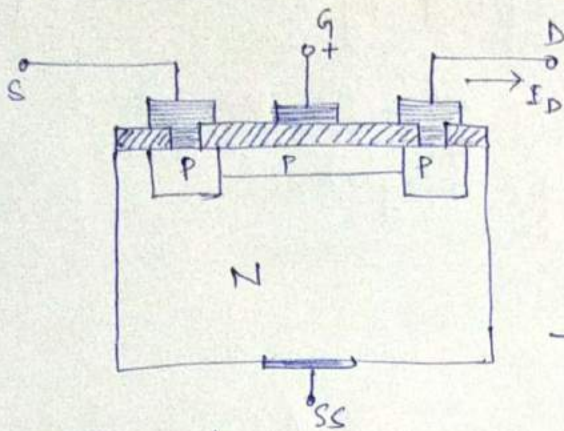
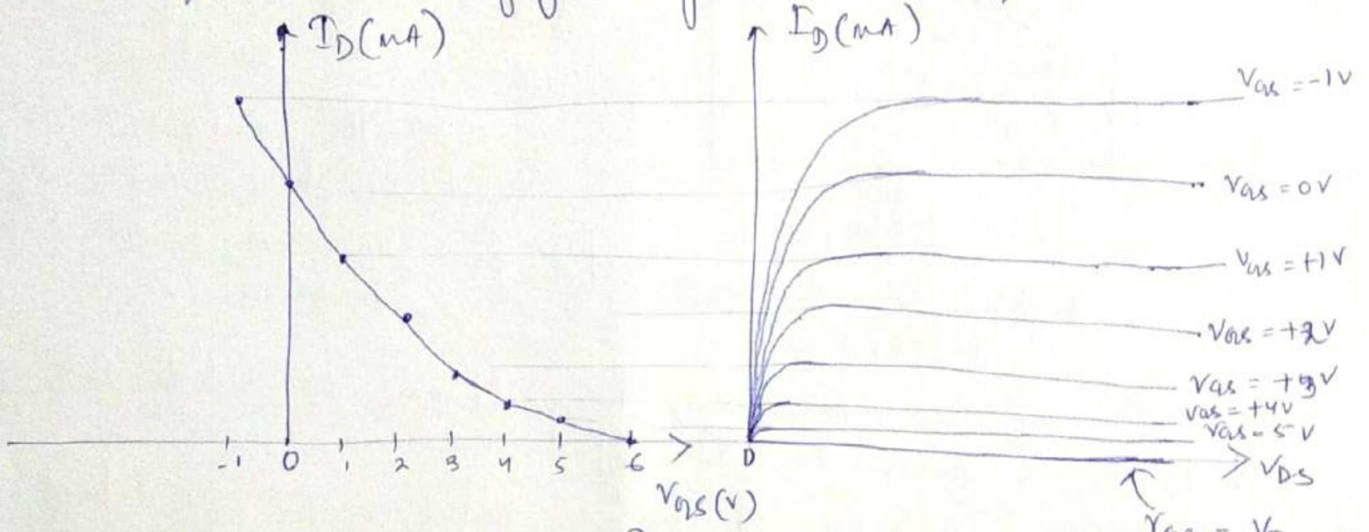
P- Channel Depletion - Type MOSFET



The construction of a p-channel depletion type MOSFET is reverse of that of N-channel MOSFET.

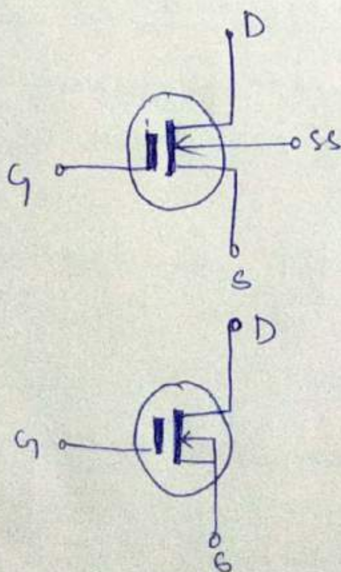
→ There is N-type substrate and p-type channel.

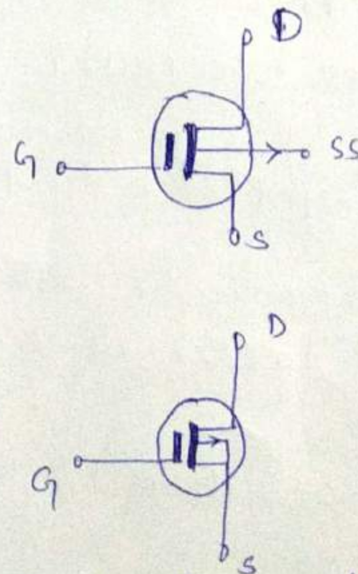
→ The drain current increases from cutoff at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and continues to increase for increasingly negative values of V_{GS}.



(Transfer characteristic) (drain characteristic)

Graphic Symbol





(N- channel depletion type MOSFET)

(P- channel depletion type MOSFET)

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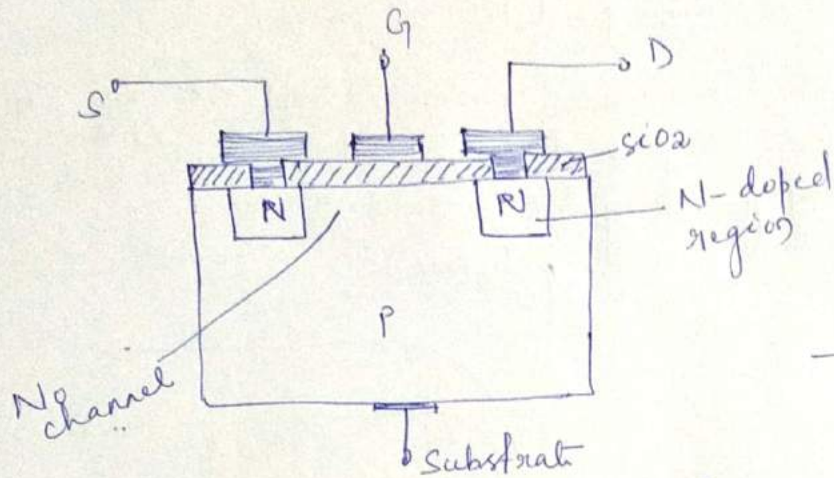
Enhancement - Type MOSFET

→ The transfer curve is not defined by the Schockley's equation.

→ The drain current I_D is cut-off until the gate-to-source voltage V_{GS} reaches a specific magnitude.

Basic construction



(N-channel enhancement-type MOSFET)

→ A slab of p-type material is formed from a silicon base and is referred to as the substrate.

→ The substrate is sometimes internally connected to the source terminal.

→ The source and drain terminals are connected through metallic contacts to N-doped regions.

→ There is absence of channel between the N doped regions.

Three major differences between Depletion-type and Enhancement-type MOSFET

Depletion-type MOSFET	Enhancement-type MOSFET
i) Presence of channel between the two N-doped or p-doped regions.	i) Absence of channel between the two N-doped or p-doped regions.
ii) Transfer characteristic curve is defined by Schockley's equation.	ii) Transfer characteristic curve is not defined by Schockley's equation.
iii) When $V_{GS} = 0V$, ~~drain~~ I_D still flows.	iii) I_D is 0mA, until V_{GS} ~~step~~ reaches a specific magnitude.

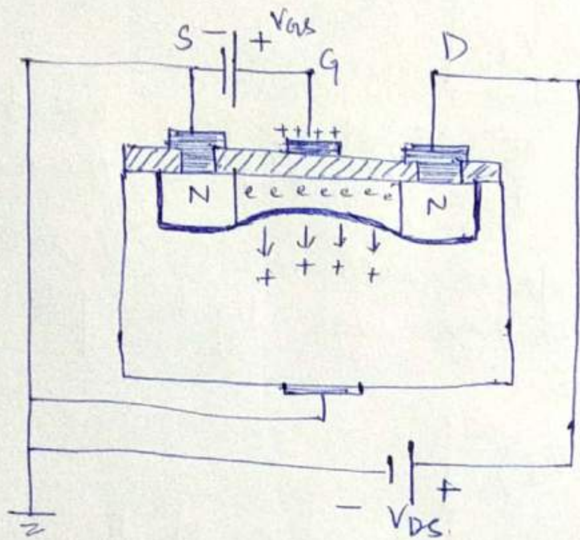
Basic operation (N-channel Enhancement-type MOSFET)

Case-I ($V_{GS} = 0V$, $V_{DS} > 0V$)

→ If V_{GS} is set at 0V, and a voltage applied between the drain and source of the device, the absence of an N-channel results in a current of zero ampere.

→ With $V_{DS} > 0V$, $V_{GS} = 0V$ and terminal SS directly connected to the source, there are two reverse-biased P-N junctions between the N-doped regions and the P-substrate opposes any significant flow between drain and source.

Case-II ($V_{GS} > 0V$, $V_{DS} > 0V$)



(Channel formation in the N-channel enhancement type MOSFET)

→ The positive potential at the gate repels the holes in the P-substrate and attracts the electrons.

→ The electrons accumulate in the region near the surface of the SiO_2 layer.

→ The SiO_2 layer and its insulating qualities prevent the negative carriers from being absorbed at the Gate terminal.

→ As V_{GS} increases in magnitude the concentration of electrons near the SiO_2 surface increases which induces the flow of current between drain and source.

→ The level of V_{GS} that results in the significant increase in drain current is called the <u>threshold voltage</u> and is given by V_T.

→ Since the channel is absent at $V_{GS} = 0V$ and enhanced by the application of positive V_{GS}, this type of MOSFET is called an enhancement-type MOSFET.

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Case-III ($V_{GS} > 0V$, but constant, V_{DS} increases)

→ If V_{GS} is constant, V_{DS} increases, gate-to-drain voltage decreases as per equation

$$V_{DG} = V_{DS} - V_{GS}$$

→ This reduces the attractive forces for free electrons in this region of the induced channel, causing a reduction in the effective channel width.

→ Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established.

→ Any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D

$$V_{DS_{sat}} = V_{GS} - V_T$$

For values of V_{GS} less than the threshold level the drain current of an enhancement-type MOSFET is 0 mA.

For levels of $V_{GS} > V_T$, the drain current I_D is related to the applied gate-to-source voltage V_{GS} by the following nonlinear relationship

$$I_D = K(V_{GS} - V_T)^2$$

where K is a constant that is a function of the construction of the device.

Then

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

Where $I_{D(on)}$ ~~not~~ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device

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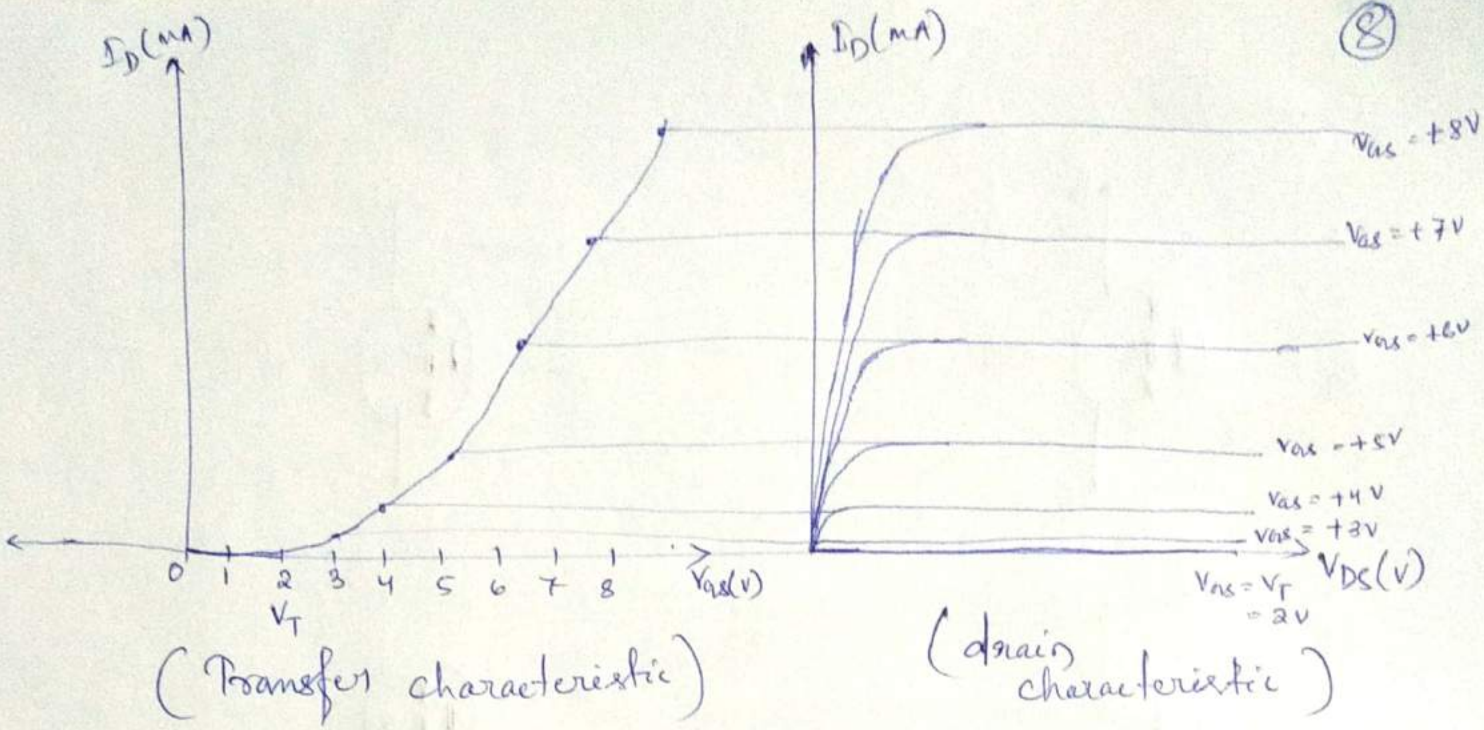
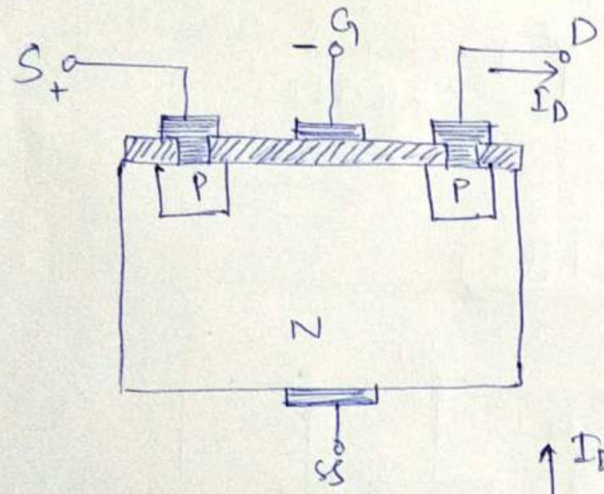
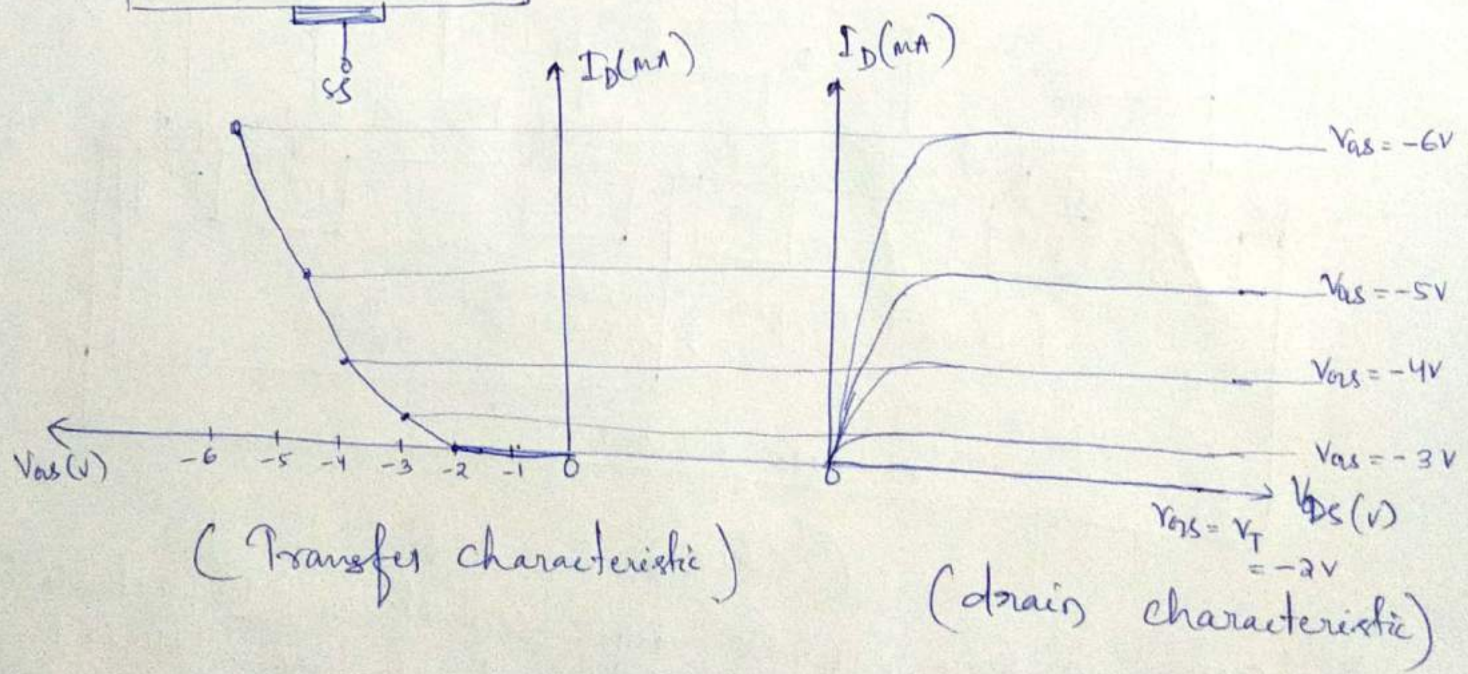


(Transfer characteristic) (drain characteristic)

P– channel Enhancement- Type MOSFETs



→ The construction of a P–channel enhancement – type MOSFET is exactly reverse of N–channel enhancement - type MOSFET.



(Transfer characteristic) (drain characteristic)

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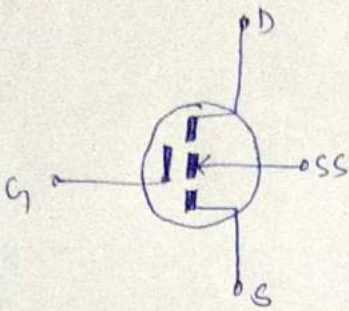
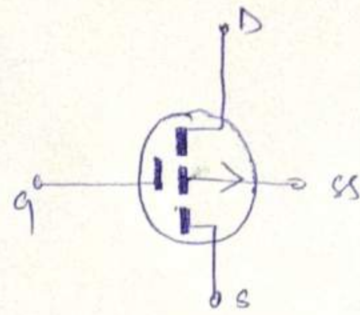
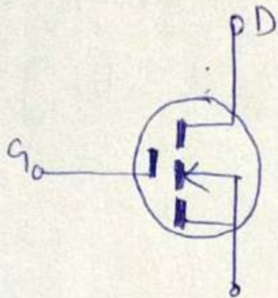
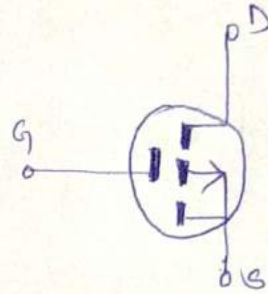
Symbols





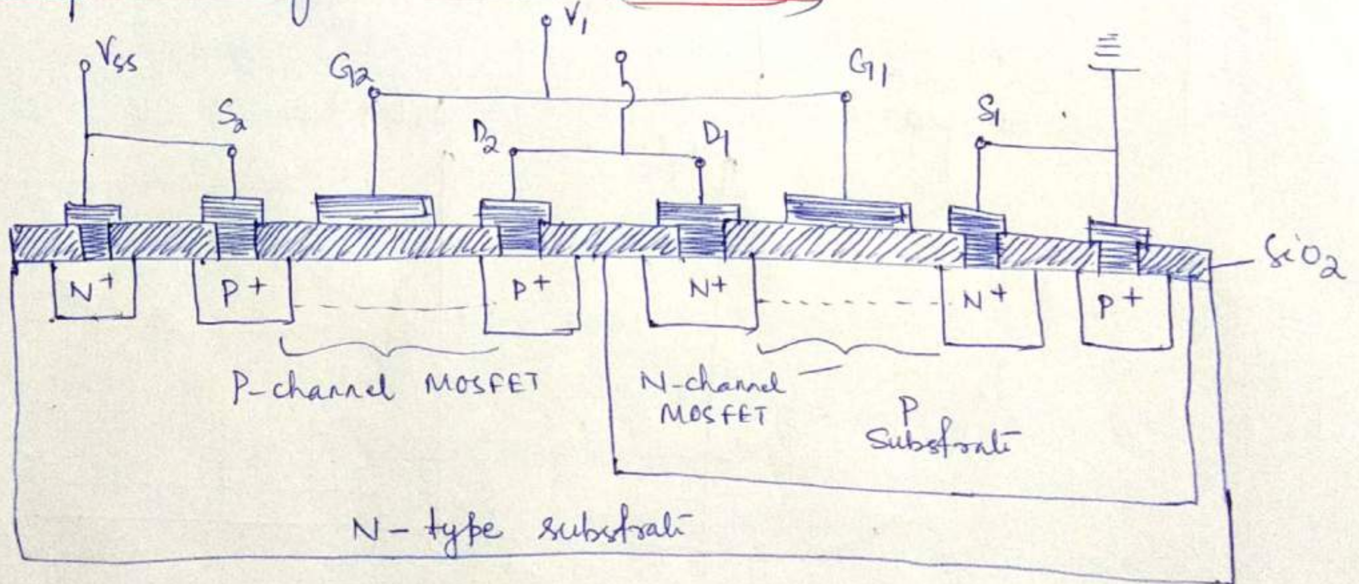




(N-channel enhancement-type MOSFET)

(P-channel enhancement-type MOSFET)

Complementary MOSFET (CMOS)



(CMOS)

→ CMOS is very effective logic circuit can be established by constructing a P-channel and N-channel MOSFET on the same substrate.

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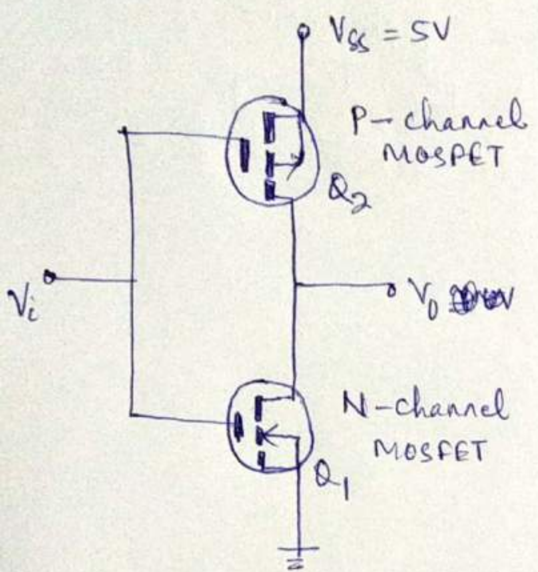
Characteristics

<i> High input impendance
<ii> Fast switching speeds
<iii> Lower operating power levels

Effective application of CMOS is an <u>inverter</u>.



(CMOS inverter)

An inverter is a logic element that inverts the applied signal.

→ As shown in the figure, gates of both P-channel and N-channel MOSFET are commonly connected to the applied voltage signal V_i.

→ Drains of both MOSFETs are connected to V_0.

→ The source of the P-channel MOSFET is connected directly to the applied voltage V_{SS} and the source of the N-channel MOSFET (Q_1) is connected to ground.

<u>As we know</u>

N-channel Enhancement MOSFET is ON → $V_{GS} \geq V_T$
P-channel " " " " → $V_{GS} \leq V_T$

So, when $V_i = 5V$, Q_1 is ON and Q_2 is OFF.
Hence Q_1 offers a very low resistance path and Q_2 induces a high resistance path or is OFF condition.
So $V_{out} = 0V$ (called 0 state)

Similarly when $V_i = 0V$, Q_1 is OFF and Q_2 is ON.
So $V_{out} = V_{SS} = 5V$ (called 1 state)

It is used in computer logic design. <u>Inverter</u>

~~V_i input | Transistor state Q_1 Q_2 | V_{out} | logic state~~

A	Y
0	1
1	0

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input $V_i(V)$	Logic state	Transistor status Q_1	Q_2	output $V_O(V)$	Logic state
5	1	ON	OFF	0	0
0	0	OFF	ON	5	1

→ Since the drain current that flows for either case is limited by the 'off' transistor to the leakage value, the power dissipated by the device in either state is very low.

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